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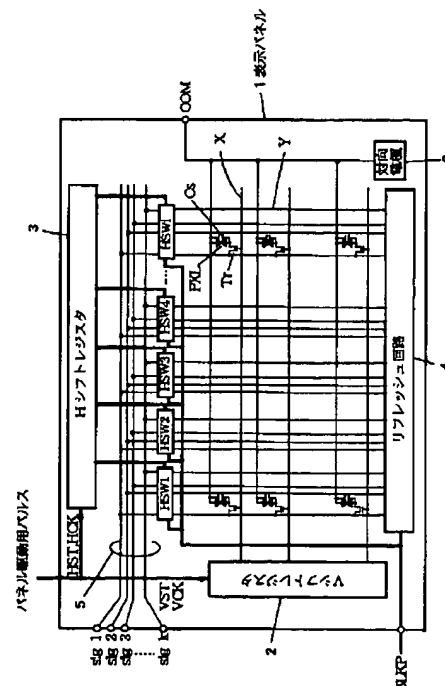
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(54) 【発明の名称】 アクティブマトリクス表示装置

(57) 【要約】

【課題】 アクティブマトリクス表示装置をパネルに用いたディスプレイシステムの全体としての消費電力を抑制する。

【解決手段】 アクティブマトリクス表示装置1は行状のゲート線Xと、列状の信号線Yと、両者の交差部に配された行列状の画素PXLと、各ゲート線Xを線順次走査し一水平期間毎に一行分の画素PXLを選択するVシフトレジスタ2と、一水平期間内で外部から供給された映像信号sig1～sigkを各信号線Yにサンプリングし選択された一行分の画素PXLに映像信号sig1～sigkの書き込みを行なうHシフトレジスタ3とを有する。更に、リフレッシュ回路4を備えており、映像信号sig1～sigkのブランキング期間に信号線Yを外部的に一時的に切り離すとともに、互いに反対極性の映像信号sig1～sigkがサンプリングされていた複数の信号線Yをブランキング期間で内部的に短絡させ、各信号線Yの電荷を外部的に切り離れた状態で内部的に中和する。



【特許請求の範囲】

【請求項1】 行状のゲート線と、列状の信号線と、両者の各交差部に配された行列状の画素と、各ゲート線を線順次走査し一水平期間毎に一行分の画素を選択する垂直駆動回路と、一水平期間内で外部から供給された映像信号を各信号線にサンプリングし選択された一行分の画素に映像信号の書き込みを行なう水平駆動回路とを有するアクティブマトリクス表示装置であって、

映像信号のブランキング期間に信号線を外部から一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線を該ブランキング期間で内部的に短絡させ各信号線の電荷を外部から切り離した状態で内部的に中和するリフレッシュ回路を有することを特徴とするアクティブマトリクス表示装置。

【請求項2】 前記リフレッシュ回路は、全信号線を外部から切り離すとともに全信号線を内部的に短絡させることを特徴とする請求項1記載のアクティブマトリクス表示装置。

【請求項3】 前記リフレッシュ回路は、全信号線を複数本ずつ組に分け組同志で短絡させることを特徴とする請求項1記載のアクティブマトリクス表示装置。

【請求項4】 前記水平駆動回路は、列状に配列した信号線に対して交互に反対極性の映像信号をサンプリングすることを特徴とする請求項1記載のアクティブマトリクス表示装置。

【請求項5】 所定の基準電圧に対して極性が反転する映像信号を供給するビデオドライバと、該映像信号に同期して制御信号を供給するタイミングジェネレータと、該制御信号に応じて動作し該映像信号に基づいて映像を表示する表示パネルとからなるディスプレイシステムであって、

前記表示パネルは、行状のゲート線と、列状の信号線と、両者の各交差部に配された行列状の画素と、各ゲート線を線順次走査し一水平期間毎に一行分の画素を選択する垂直駆動回路と、一水平期間内で外部の該ビデオドライバから供給された映像信号を各信号線にサンプリングし選択された一行分の画素に映像信号を書き込んで映像を表示する水平駆動回路とを備え、

該タイミングジェネレータから供給された制御信号に応じて映像信号のブランキング期間に信号線を外部の該ビデオドライバから一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線を該ブランキング期間で内部的に短絡させ各信号線の電荷を外部から切り離した状態で内部的に中和するリフレッシュ回路を有することを特徴とするディスプレイシステム。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】 本発明は画面を構成する画素とこれを駆動する薄膜トランジスタなどのスイッチング

素子と周辺の駆動回路とを内蔵したアクティブマトリクス表示装置（以下、表示パネルと略称する場合がある）に関する。又、所定の基準電圧に対して極性を反転する映像信号を供給するビデオドライバと、映像信号に同期して制御信号を供給するタイミングジェネレータと、制御信号に応じて動作し映像信号に基づいて映像を表示する表示パネルとからなるディスプレイシステムに関する。

【0002】

【従来の技術】 図15を参照して従来のアクティブマトリクス表示装置を簡単に説明する。図示する様に、表示パネル1は行状のゲート線Xと、列状の信号線Yとを備えており、両者の交差部に画素PXLが設けられている。画素PXLは一方の基板に形成された画素電極と、他方の基板に形成された対向電極6と、両者の間に保持された液晶などの電気光学物質とからなる。各画素PXLは対応する薄膜トランジスタTrによりスイッチング駆動される。又、各画素PXLに対応して補助容量Csも形成されている。薄膜トランジスタTrのゲート電極は対応するゲート線Xに接続され、ソース電極は対応する信号線Yに接続され、ドレイン電極は対応する画素電極に接続されている。表示パネル1はk本の入力線5を備えており、外部のビデオドライバから供給されるk個の映像信号sig1, sig2, ..., sigkをそれぞれ受け入れる。個々の信号線Yはk本を一単位として水平スイッチHSWを介して所定の入力線5に接続されている。以上の構成に加え、表示パネル1はVシフトレジスタ2とHシフトレジスタ3を内蔵している。Vシフトレジスタ2は垂直駆動回路を構成し、外部のタイミングジェネレータから供給される垂直スタートパルスVSTや垂直クロックパルスVCKなどのパネル駆動用パルスにตอบสนองして動作し、ゲート線Xを一本ずつ順次走査して画素を行毎に選択する。一方、Hシフトレジスタ3は同じくタイミングジェネレータから供給される水平スタートパルスHSTや水平クロックパルスHCKなどのパネル駆動用パルスにตอบสนองして動作し、順次サンプリングパルスを出力し対応する水平スイッチHSW1, HSW2, ..., HSWiを開閉制御して、k本の信号線Yを一単位としてまとめ駆動する。即ち、k系統の映像信号sig1, ..., sigkをそれぞれ対応する信号線Yに一斉サンプリングする。

【0003】 係る複数画素同時サンプリング駆動を行なう際、k系統の映像信号sig1～sigkにあらかじめ画素ピッチに対応する遅延量を相対的に与える為、サンプルホールド回路がビデオドライバに設けられている。k系統の映像信号を逐次サンプルホールドして画素ピッチに対応する遅延量を相対的に与えるとともに、水平スイッチHSWをk本の信号線の組を単位として同時に開閉制御することにより、この水平スイッチを駆動するHシフトレジスタ3に含まれる段数を削減して構成を

簡単にすることができる。なお、HSW1～HSWiとHシフトレジスタ3とで水平駆動回路を構成する。

【0004】図16は、従来のディスプレイシステムの全体構成を示すブロック図である。ディスプレイシステムはビデオドライバ8と、図15に示した表示パネル1と、タイミングジェネレータ(TG)9とを備えている。なお、表示パネル1は電気光学物質として液晶(LC)を用いる場合が多いので、ここではLCDと呼ぶ場合がある。ビデオドライバ8は外部入力されるビデオ信号SIGを処理してLCD1の駆動に適した映像信号sigに変換する。例えば、ビデオドライバ8は一水平期間(1H)で映像信号sigの極性反転処理を行ない、交流化された映像信号sigをLCD1に出力する。LCD1は図15に示した通り、行状のゲート線、列状の信号線、及び両者の交差部に設けた液晶画素を備えている。又、垂直駆動回路及び水平駆動回路を内蔵している。垂直駆動回路はゲート線を順次走査して画素を選択する。水平駆動回路は1H毎に交流化映像信号sigを信号線に順次サンプリングし、選択された画素に交流化映像信号sigを書き込む。タイミングジェネレータ9は同期信号SINCに応じて動作し、ビデオドライバ8に対し交流化信号FRPを供給して極性反転処理のタイミング制御を行なう。又、ビデオドライバ8に対しサンプルホールド信号SHPを供給し、映像信号sigの遅延処理を制御している。即ち、ビデオドライバ8は画素の配列ピッチに応じ複数系統の映像信号sigを相対的に遅延処理してLCD1に供給している。タイミングジェネレータ9は更に、HST、HCK、VST、VCKなどのパネル駆動用パルスをLCD1に供給し、垂直駆動回路及び水平駆動回路の動作制御を行なう。

【0005】ビデオドライバ8は、例えばクランプ回路CLP、ブライツ回路BRT、ガンマ補正回路 γ 、ゲイン回路GAIN、反転回路INV、AMP、極性反転スイッチSW、サンプルホールド回路S/H、負荷駆動用バッファBUFFなどで構成されている。

【0006】図17を参照して、図16に示したディスプレイシステムの動作を簡潔に説明する。外部から入力されたビデオ信号SIGはクランプ回路CLPでベデスタルクランプされ、基準となる電圧が決められる。ベデスタルクランプされた信号は、ブライツ回路BRTで輝度を調整する為にブライツコントロールされる。ブライツコントロールされた信号はガンマ補正回路 γ でLCD1の特性に合わせた γ 補正を行なう。 γ 補正された信号はゲイン回路GAINでゲイン調整を施される。ゲイン調整された信号AMPINは極性反転スイッチSWによって交流化される。この極性反転スイッチSWはタイミングジェネレータ9から供給されるFRPによりオン/オフ制御される。交流化された信号は複数画素同時駆動を採用するLCD1に適した位相差を付ける為、サンプルホールド回路S/Hを通る。なお、このサンプルホー

ルド回路S/Hはタイミングジェネレータ9から供給されるSHPにより制御されている。サンプルホールドされた映像信号sigはバッファBUFFを介してLCD1に供給される。前述した様に、複数系統の映像信号sig1～sigkは順次開閉制御されるHSW1～HSWiによってkドット毎同時に画素に書き込まれる。なお、図17から明らかな様に、LCD1に供給される映像信号sigは1H毎に所定の基準電圧に対して極性が反転している。この基準電圧は図15に示した対向電極6に印加される共通電圧COMにほぼ等しい。

【0007】図18は、LCD1の各画素PXLに書き込まれる映像信号sigの極性を模式的に表わしている。この例では、 $k=6$ として、6画素毎同時に6系統の映像信号sig1～sig6が書き込まれる。なお、画素PXLは全体としてn行m列のマトリクスを構成している。本例は、所謂ドット反転駆動を採用している。ゲート線X1に対応する1ライン目では、信号線Y1～Y6を介して6個の画素1-1, 1-2, 1-3, 1-4, 1-5, 1-6に+-+-+-の極性の映像信号sig1～sig6が書き込まれる。次の2ライン目では、画素2-1, 2-2, 2-3, 2-4, 2-5, 2-6に、-+-+-+の極性の映像信号sig1～sig6が書き込まれる。この様に、ドット反転駆動では、 $n \times m$ の画素PXLに対して互いに反対極性の映像信号sigが千鳥状に書き込まれる。

【0008】

【発明が解決しようとする課題】以上の様に、通常LCD1は液晶の劣化を防ぐ為交流駆動が必要であり、映像信号sigを共通電圧COMに対して反転する必要がある。この為、例えば共通電圧COMに対して最大 V_{max} の電圧を画素PXLに書き込む場合には、極性反転毎に最大で $2V_{max}$ の電圧を遷移させる必要がある。従って、短時間の間に最大で $2V_{max}$ の電圧を遷移させることができる能力を備えたバッファBUFFが外部のビデオドライバ8に必要となる。従来のLCDを用いたディスプレイシステムでは、このバッファBUFF及び画素PXLや信号線Yなどの負荷を充放電する為に大量の電流が流れており、これがディスプレイシステムの消費電力の大半を占めていた。

【0009】この問題を解決する為、充放電の対象となる画素や信号線の負荷を軽減したり、画素に印加する電圧を低減化していた。しかしながら、前者の場合には物理的な限界があり、必ずしも充分な対策とはならない。又、後者の場合はコントラストの低下など画質劣化の副作用が現われていた。

【0010】

【課題を解決する為の手段】上述した従来の技術の課題を解決する為に以下の手段を講じた。即ち、本発明に係るアクティブマトリクス表示装置(表示パネル)は、基本的な構成として、行状のゲート線と、列状の信号線

と、両者の各交差部に配された行列状の画素と、各ゲート線を線順次走査し一水平期間毎に一行分の画素を選択する垂直駆動回路と、一水平期間内で外部から供給された映像信号を各信号線にサンプリングし選択された一行分の画素に映像信号の書き込みを行なう水平駆動回路とを有する。特徴事項として、本アクティブマトリクス表示装置はリフレッシュ回路を備えており、映像信号のブランキング期間に信号線を外部から一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線を該ブランキング期間で内部的に短絡させ、各信号線の電荷を外部から切り離した状態で内部的に中和する。好ましくは、前記リフレッシュ回路は、全信号線を外部から切り離すとともに、全信号線を内部的に短絡させる。あるいは、前記リフレッシュ回路は、全信号線を複数本づつ組に分け組同志で短絡させてもよい。なお、前記水平駆動回路は、例えば列状に配列した信号線に対して交互に反対極性の映像信号をサンプリングする。

【0011】本発明は、上述したアクティブマトリクス表示装置を表示パネルに用いたディスプレイシステムを包含している。本ディスプレイシステムは基本的な構成として、所定の基準電圧に対して極性が反転する映像信号を供給するビデオドライバと、該映像信号に同期して制御信号を供給するタイミングジェネレータと、該制御信号に応じて動作し該映像信号に基づいて映像を表示する表示パネルとからなる。前記表示パネルは、行状のゲート線と、列状の信号線と、両者の各交差部に配された行列状の画素と、各ゲート線を線順次走査し一水平期間毎に一行分の画素を選択する垂直駆動回路と、一水平期間内で外部の該ビデオドライバから供給された映像信号を各信号線にサンプリングし選択された一行分の画素に映像信号を書き込んで映像を表示する水平駆動回路とを備えている。特徴事項として、本表示パネルはリフレッシュ回路を内蔵しており、該タイミングジェネレータから供給された制御信号に応じて映像信号のブランキング期間に信号線を外部の該ビデオドライバから一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線を該ブランキング期間で内部的に短絡させ、各信号線の電荷を外部から切り離した状態で内部的に中和する。

【0012】通常、LCDなどの表示パネルは映像信号を基準電圧に対して反転する為、画素に書き込む電圧の2倍を充放電する必要がある。本発明では、ブランキング期間にLCD内部で正極性の映像信号がサンプリングされた信号線と負極性の映像信号がサンプリングされた信号線を互いに短絡（ショート）し、電荷を中和（キャンセル）している。これにより、有効期間に充放電する電荷を減らし、ディスプレイシステムの低消費電力化を図っている。具体的には、アクティブマトリクス表示パネルにおいて、例えばドット反転駆動を採用した場合、

一水平期間毎の映像ブランキング期間に、全信号線をショートさせることによって、パネル内の信号線を一度基準電圧付近の電圧にリフレッシュする。この時、表示パネル内の信号線と外部のビデオドライバは完全に分離することにより、パネル内部の電荷のみでリフレッシュする。あるいは、ドット反転駆動において、一水平期間毎の映像ブランキング期間に、隣り合う複数本の信号線毎にそれぞれショートさせることによって、表示パネル内の信号線を基準電圧付近の電圧にリフレッシュすることも可能である。従来の表示パネルではビデオドライバ側で基準電圧に対して負極性側から正極性側あるいは正極性側から負極性側に信号線を充放電していた。本発明によれば、パネル内部の電荷のみで信号線の電位を基準電圧付近にリフレッシュできる為、外部回路からの充放電を大幅に削減することができ、ディスプレイシステム全体での消費電力を低減化可能である。本発明によれば、負荷を削減したり画素に書き込む電圧を低減化することなしに、低消費電力化を達成することが可能である。

【0013】

【発明の実施の形態】以下図面を参照して本発明の実施形態を詳細に説明する。図1は、本発明に係るアクティブマトリクス表示装置（表示パネル）の基本的な構成を示す回路図である。なお、図15に示した従来のアクティブマトリクス表示装置と対応する部分には対応する参照番号を付して理解を容易にしている。本実施形態は、所謂複数画素同時駆動方式を採用している。但し、本発明はこれに限られるものではなく、画素1個毎に映像信号を書き込む点順次方式あるいは一行分の画素に一括で映像信号を書き込む線順次方式にも適用可能である。図示する様に、表示パネル1は行状のゲート線Xと、列状の信号線Yとを備えており、両者の交差部に画素PXLが設けられている。各画素PXLは対応する薄膜トランジスタTrによりスイッチング駆動される。薄膜トランジスタTrのゲート電極は対応するゲート線Xに接続され、ソース電極は対応する信号線Yに接続され、ドレイン電極は対応する画素電極に接続されている。各画素電極は対向電極6に対面しており、両者の間に液晶などの電気光学物質が保持されている。対向電極6には外部から共通電圧COMが印加されている。表示パネル1はk本の入力線5を備えており、外部のビデオドライバから供給されるk個の映像信号sig1～sigkをそれぞれ受け入れる。個々の信号線Yはk本を一単位として水平スイッチHSWを介して所定の入力線5に接続されている。以上の構成に加え、表示パネル1はVシフトレジスタ2とHシフトレジスタ3を内蔵している。Vシフトレジスタ2は外部のタイミングジェネレータから供給される垂直スタートパルスVSTや垂直クロックパルスVCKなどのパネル駆動用パルスにตอบสนองして動作し、ゲート線Xを一本づつ順次走査して画素を行毎に選択する。即ち、Vシフトレジスタ2は垂直駆動回路を構成する。

一方、Hシフトレジスタ3は同じくタイミングジェネレータから供給される水平スタートパルスHSTや水平クロックパルスHCKなどのパネル駆動用パルスにตอบสนองして動作し、順次サンプリングパルスを出力し対応する水平スイッチHSW1～HSWiを開閉制御して、k本の信号線Yを一単位としてまとめ駆動する。即ち、k系統の映像信号sig1～sigkをそれぞれ対応する信号線Yに一斉サンプリングする。Hシフトレジスタ3とHSWとで水平駆動回路を構成する。

【0014】特徴事項として、本表示パネル1はリフレッシュ回路4を備えている。このリフレッシュ回路4は外部のタイミングジェネレータから供給される制御信号BLKPに応じて動作し、映像信号sig1～sigkのブランキング期間に信号線Yを外部のビデオドライバから一時的に切り離すとともに、互いに反対極性の映像信号sig1～sigkがサンプリングされていた複数の信号線Yをブランキング期間で内部的に短絡させ、各信号線Yの電荷を外部から切り離した状態で内部的に中和する。具体的には、リフレッシュ回路4はBLKPに応じて水平スイッチHSW1～HSWiをブランキング期間中一時的にオフ状態にするとともに、リフレッシュ回路4の本体内で各信号線Yを電気的に接続する。

【0015】図2はリフレッシュ回路4の具体的な構成例を示す。(A)に示した例では、全信号線Yを外部から切り離すとともに、BLKPに応じて全信号線Yを内部的に短絡させる為のスイッチRSWを備えている。一方(B)の例では、信号線Yを例えばk本づつ組に分け、2組づつ互いに短絡させている。なお、本発明はこれに限られるものではなく、基本的に正極性の映像信号がサンプリングされた信号線と負極性の映像信号がサンプリングされた信号線を、同数本づつ短絡させればよい。

【0016】図3は、本発明に係るディスプレイシステムを示すブロック図である。なお、理解を容易にする為、図16に示した従来のディスプレイシステムと対応する部分には対応する参照番号を付している。図示する様に、本ディスプレイシステムはビデオドライバ8とタイミングジェネレータ9と表示パネル(LCD)1とを備えている。ビデオドライバ8は所定の基準電圧に対して極性反転する映像信号sigを供給する。タイミングジェネレータ9は映像信号sigに同期してパネル駆動用パルスや制御信号BLKPを供給する。LCD1はパネル駆動用パルスや制御信号BLKPに応じて動作し映像信号sigに基づいて映像を表示する。前述した様に、LCD1は行状のゲート線と、列状の信号線と、両者の各交差部に配された行列状の画素と、各ゲート線を線順次走査し一水平期間毎に一行分の画素を選択する垂直駆動回路と、一水平期間内で外部のビデオドライバ8から供給された映像信号sigを各信号線にサンプリングし選択された一行分の画素に映像信号を書き込んで映

像を表示する水平駆動回路とを備えている。なお、垂直駆動回路はVシフトレジスタから構成されており、水平駆動回路はHシフトレジスタと水平スイッチHSWとの組合わせて構成されている。特徴事項として、LCD1はリフレッシュ回路を内蔵している。このリフレッシュ回路はタイミングジェネレータ9から供給される制御信号BLKPに応じて映像信号sigのブランキング期間に信号線を外部のビデオドライバ8から一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線をブランキング期間で内部的に短絡させ、各信号線の電荷を外部から切り離した状態で内部的に中和する。

【0017】図4は、本発明に係るディスプレイシステムの実施例を示すブロック図である。本実施例は6画素同時駆動方式(k=6)を採用し且つドット反転駆動方式を採用している。ビデオドライバ8はビデオ信号SIGを処理して6系統の映像信号sig1～6をLCD1に供給する。sig1～6は交流化されており且つ位相調整が施されている。sig1及びsig2には例えば赤色の映像信号が割り当てられており、sig3及びsig4には緑色の映像信号が割り当てられており、sig5及びsig6には青色の映像信号が割り当てられている。タイミングジェネレータ9は同期信号SYNCに応じて動作し、ビデオドライバ8に交流化信号FRP及びサンプルホールド信号SHPを供給している。又、タイミングジェネレータ9はLCD1に対してHST、HCK、VST、VCKなどのパネル駆動用パルスと制御信号BLKPを供給している。

【0018】図5は、図4に示した各映像信号の極性を模式的に表わしている。ビデオ信号sigは一水平期間(1H)毎に有効期間とそれ以外のブランキング期間を含んでいる。有効期間内に一行分の画素に対応した薄膜トランジスタのゲートが開き、信号線を介して各画素に映像信号が書き込まれる。映像信号sig1、sig3及びsig5は基準電圧に対して1H毎に極性が反転する。この基準電圧はLCD1の対向電極に供給される共通電圧COMと実質的に等しい。同様に、映像信号sig2、sig4及びsig6も1H毎に極性が反転する。但し、sig1、3、5とsig2、4、6は互いに反対極性となっている。例えば、一行目(1ライン目)に着目すると、sig1、3、5はCOMに対して+Vの電圧を有し、sig2、4、6はCOMに対して-Vの電圧を有する。

【0019】図6は、図4に示したLCD1の具体的な構成を示す回路図である。図示する様に、画素PXLはn行×m列のマトリクス配置になっている。合計でn本のゲート線Xは図示しないがVシフトレジスタに接続されている。又、合計でm本の信号線YはHSWを介して6本の入力線5に接続されており、それぞれsig1～sig6がサンプリングされる。各HSWはHシフトレ

ジスタ3により開閉制御される。本例では6画素同時駆動方式を採用している為、HSWの個数は $m/6$ となる。各HSWには切り離し用のスイッチCSWが内蔵されており、制御信号BLKPに応じて各HSWをオフ状態にし、信号線Yと入力線5を互いに切り離す。又、各信号線Yの他端側にはRSWを内蔵したリフレッシュ回路4が接続されている。このリフレッシュ回路4はBLKPに応じて全てのRSWをオン状態とし、全ての信号線Yを互いに短絡させる。

【0020】次に、図7ないし図10を参照して図6に示したLCDの動作を詳細に説明する。まず図7に示す様に、1ライン目につながる薄膜トランジスタTrを全てオンすることにより、1ライン目の画素1-1~1-mは全て対応する信号線Yに電気的に接続される。この時、各HSWに内蔵したCSWは全てHシフトレジスタ3側に投入されている。まず、Hシフトレジスタ3の制御によりHSW1が導通状態となり、HSW1につながる6本の信号線Y1~Y6を介して、画素1-1~1-6に一度に映像信号sig1~sig6の信号電位が書き込まれる。この結果、画素1-1, 1-2, 1-3, 1-4, 1-5, 1-6はそれぞれ+-+-+-の極性となる。次いでHSW1が開き、画素1-1~1-6に書き込まれた電位はホールドされる。この時、HSW1につながる6本の信号線Y1~Y6も対応する画素1-1~1-6と同様な極性の信号電位にホールドされる。

【0021】次に図8に示す様に、HSW2が導通状態となり、信号線Y7~Y12を介して画素1-7~1-12に+-+-+-の極性の信号電位が書き込まれる。次いでHSW2が非導通状態となり、画素1-7~1-12及びこれらにつながる信号線Y7~Y12に図示の極性の信号電位がホールドされる。この様にして、6画素毎に画素と信号線に所定の映像信号sig1~sig6が書き込まれホールドされていく。1ライン目の画素1-1~1-mの全てに信号電位が書き込まれると、1ライン目の薄膜トランジスタTrが全て非導通状態となり、一行分の走査は完了する。

【0022】この様にして一水平期間の内の有効期間が終了しブランキング期間に入る。この時、図9に示す様にタイミングジェネレータから制御信号BLKPが入力し、CSWを介して全てのHSWがオフ状態に置かれる。同時に、リフレッシュ回路4内の全てのRSWがオン状態となり、全信号線Yが互いにショートされる。即ち、+Vにチャージされていた奇数列の信号線と-Vにチャージされていた偶数列の信号線が互いに短絡状態となり、全信号線Yは±0付近の電位(COM)になる。この時、HSWは全てオフ状態となっているので、LCD外部からの電流の出入りは一切ない。+Vにチャージされている信号線と-Vにチャージされている信号線がショートされることによって、信号線は全て同電位(COM付近)にリフレッシュされる。

【0023】次に図10に示す様に、2ライン目の走査が始まる。この時には、ビデオドライバから、1ライン目とは逆極性となるsig1~sig6が供給される。即ち、sig1, 3, 5はCOMに対して-Vの電位を有し、sig2, 4, 6はCOMに対して+Vの電位となる。2ライン目に対応した薄膜トランジスタTrが導通状態になる。この後、HSWが順次開閉制御され、sig1~sig6は対応する信号線Yを介して対応する画素に書き込まれる。即ち、sig1, 3, 5がサンプリングされた信号線は電位が0から-Vに移行し、sig2, 4, 6がサンプリングされた信号線は電位が0から+Vに移行する。信号線はあらかじめ全て共通電圧付近にリフレッシュされている為、外部のビデオドライバは各信号線にVだけチャージあるいはディスチャージすればよい。従って、ビデオドライバ内のバッファで消費される電力は従来と比べ大幅に削減可能である。

【0024】上述した実施例はドット反転駆動の場合であるが、本発明はこれに限られるものではない。基本的に、ある時間に着目してLCDの共通電圧に対して、正極性にホールドされている画素及び信号線と、負極性にホールドされている画素及び信号線が存在すれば、駆動方法によらず本発明は適用可能である。例えば、列毎交互に反対極性の映像信号をサンプリングするコラム反転駆動にも適用可能である。又、行毎に極性が反転する1H反転においても、例えば一垂直ブランキング期間にリフレッシュを行なうことができる。一垂直ブランキング期間に、全ゲート線につながる薄膜トランジスタをオン状態におくとともに、全信号線を互いに短絡させることで、所望のリフレッシュを行なうことが可能である。

【0025】図11は、アクティブマトリクス表示装置の参考例を示すブロック図である。図6に示した実施例と対応する部分には対応する参照番号を付して理解を容易にしている。この参考例はリフレッシュ機能を備えていない。

【0026】続いて図12~図14を参照して、図11に示した参考例の動作を簡潔に説明する。まず図12に示す様に、1ライン目につながる薄膜トランジスタTrが全て導通状態となることにより、1ライン目の画素1-1~1-mは全て信号線Yにつながる。次いで、HSW1が閉じることにより、これにつながる6本の信号線Y1~Y6を介して、画素1-1~1-6に一度に信号電位が書き込まれる。次いでHSW1が開き、画素1-1~1-6に書き込まれた電位はホールドされる。この時、HSW1につながる6本の信号線Y1~Y6も、画素と同様に信号電位がホールドされる。即ち、信号線Y1, Y3, Y5は+Vにチャージされ、信号線Y2, Y4, Y6は-Vにチャージされる。

【0027】続いて図13に示す様に、HSW2が導通状態となり、画素1-7~1-12に信号電位が書き込まれる。この後、HSW2が非導通状態となり、画素1

11

ー7～1-12と信号線Y7～Y12に信号電位がホールドされる。Y7, Y9, Y11は+Vにホールドされ、Y8, Y10, Y12は-Vにホールドされる。以下同様にして、6画素毎に画素と信号線に信号電位が書き込まれホールドされていく。1ライン目の画素1-1～1-mに全て信号電位が書き込まれると、1ライン目の薄膜トランジスタ(画素スイッチ)Trが全てオフ状態となり、1ライン目の走査は完了する。

【0028】この後図14に示す様に、ビデオドライバから1ライン目とは逆極性の映像信号sig1～sig6が供給される。sig1, 3, 5はCOMに対して負極性の電位となり、sig2, 4, 6はCOMに対して正極性の電位となる。次いで、2ライン目の薄膜トランジスタTrがオン状態となった後、HSWが順次開閉制御され、sig1～sig6が各信号線を介して画素に書き込まれていく。信号線Y1, Y3, Y5に着目すると、1ライン目では+Vにホールドされていた電位が2ライン目では-Vに書き換えられる。この時、ビデオドライバ側のバッファは2Vのディスチャージを行わなければならない。又信号線Y2, Y4, Y6に着目すると、1ライン目では-Vにホールドされていた電位が2ライン目では+Vに書き換えられる。この時、ビデオドライバ側のバッファは2Vのチャージを行わなければならない。この様に、ビデオドライバ内のバッファは大きな電力を消費する。

【0029】

【発明の効果】以上説明したように、本発明によれば、アクティブマトリクス表示装置はリフレッシュ回路を内蔵しており、映像信号のブランキング期間に信号線を外部から一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線をブランキング期間で内部的に短絡させ、各信号線の電荷を外部から切り離した状態で内部的に中和する。従来のアクティブマトリクス表示装置では、外部と接続した状態で信号線の電位を共通電圧(基準電圧)に対して負側から正側、あるいは正側から負側に充放電していた。これに対し、本発明を用いれば、アクティブマトリクス表示装置内部の電荷のみで信号線電位を共通電圧付近にリフレッシュできる為、外部回路からの充放電を大幅に減らすことができ、ディスプレイシステム全体での消費電力を削減することが可能である。

【図面の簡単な説明】

12

【図1】本発明に係るアクティブマトリクス表示装置の実施形態を示す回路図である。

【図2】図1に示した実施形態に含まれるリフレッシュ回路の具体的な構成を示す回路図である。

【図3】本発明に係るディスプレイシステムの全体構成を示すブロック図である。

【図4】本発明に係るディスプレイシステムの実施例を示すブロック図である。

【図5】図4に示した実施例の動作説明に供するタイミングチャートである。

【図6】図4に示した実施例に含まれるアクティブマトリクス表示装置の具体的な構成を示す回路図である。

【図7】図6に示したアクティブマトリクス表示装置の動作説明に供する回路図である。

【図8】図6に示したアクティブマトリクス表示装置の動作説明に供する回路図である。

【図9】図6に示したアクティブマトリクス表示装置の動作説明に供する回路図である。

【図10】図6に示したアクティブマトリクス表示装置の動作説明に供する回路図である。

【図11】アクティブマトリクス表示装置の参考例を示す回路図である。

【図12】図11に示した参考例の動作説明に供する回路図である。

【図13】図11に示した参考例の動作説明に供する回路図である。

【図14】図11に示した参考例の動作説明に供する回路図である。

【図15】従来のアクティブマトリクス表示装置の一例を示す回路図である。

【図16】従来のディスプレイシステムの一例を示すブロック図である。

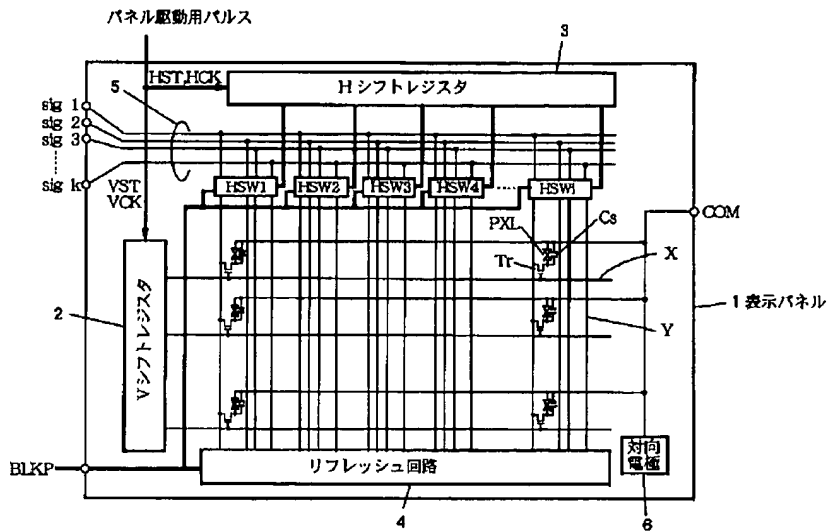
【図17】図16に示した従来のディスプレイシステムの動作説明に供する波形図である。

【図18】図15に示した従来のアクティブマトリクス表示装置の動作説明に供する模式図である。

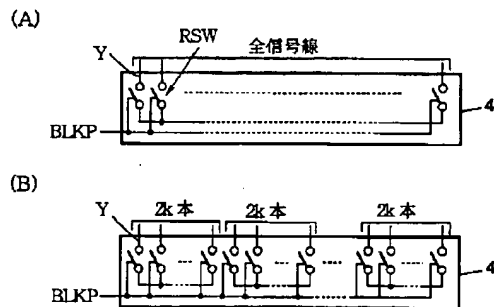
【符号の説明】

1・・・表示パネル、2・・・Vシフトレジスタ、3・・・Hシフトレジスタ、4・・・リフレッシュ回路、5・・・入力線、6・・・対向電極、8・・・ビデオドライバ、9・・・タイミングジェネレータ

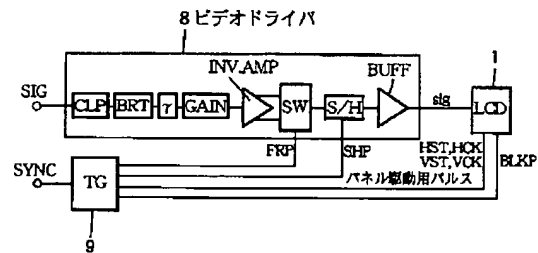
【図1】



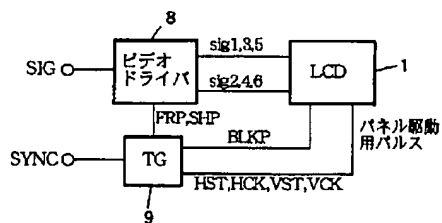
【図2】



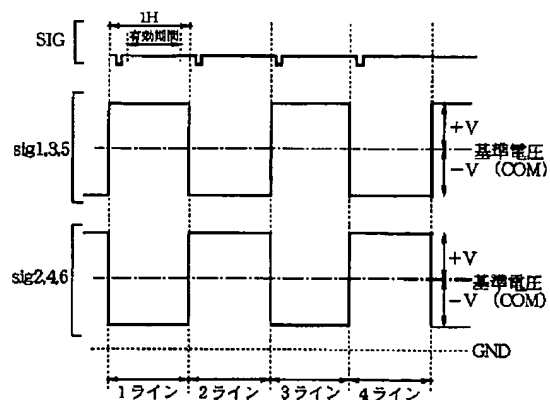
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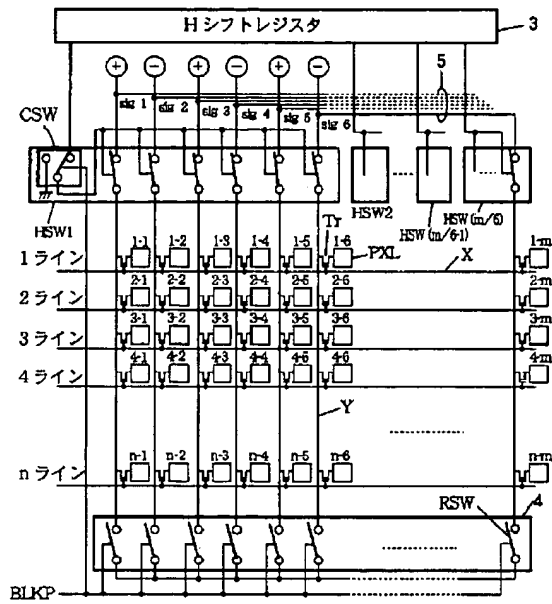
【図4】



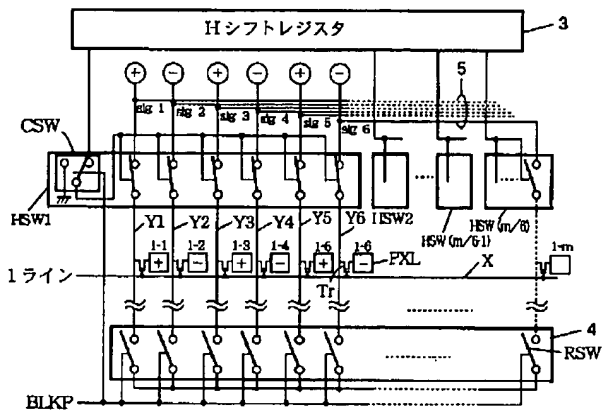
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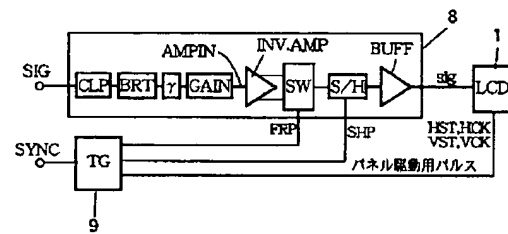
【図6】



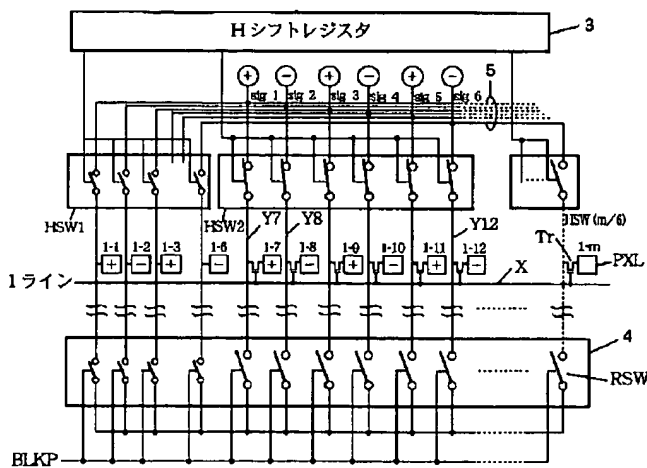
【図7】



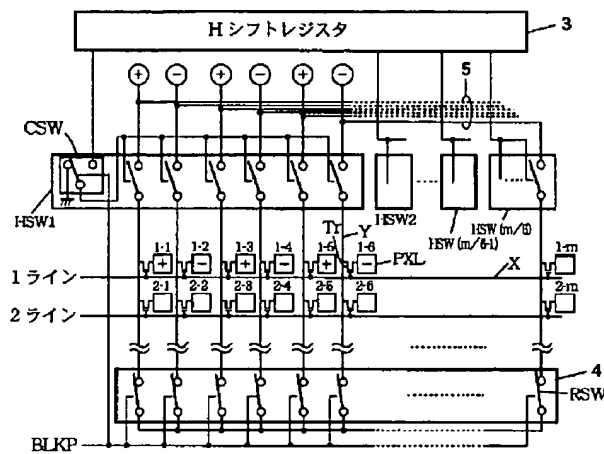
【図16】



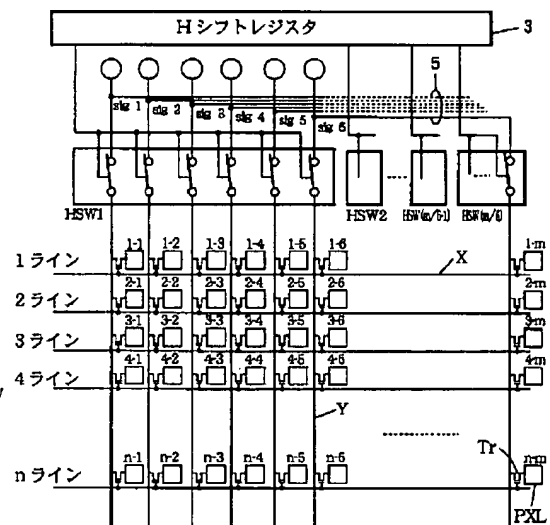
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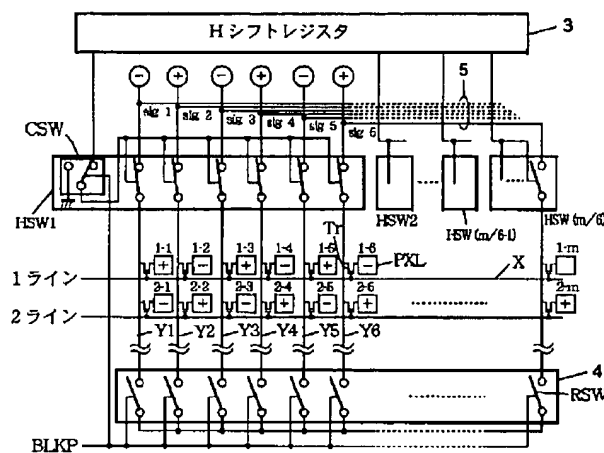
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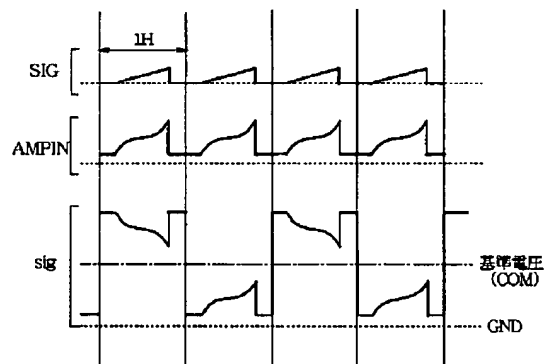
【図11】



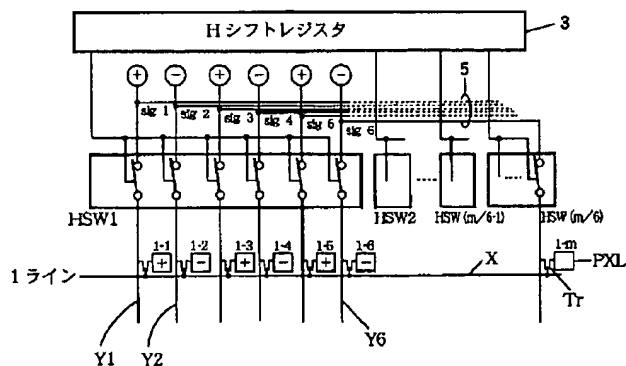
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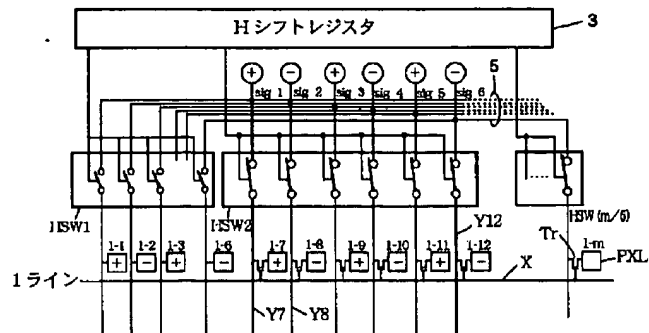
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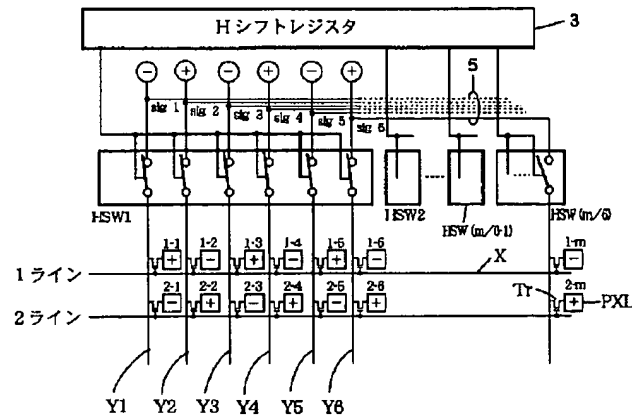
【図12】



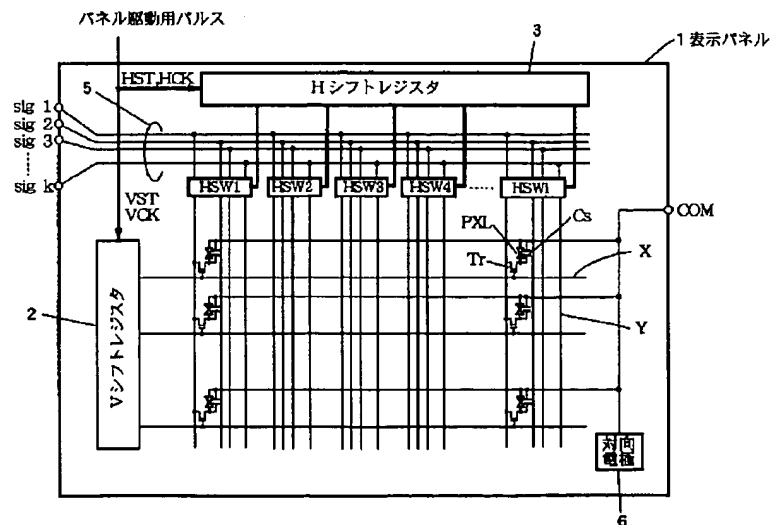
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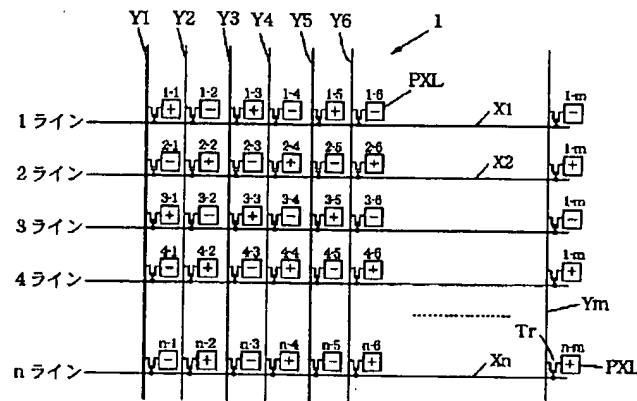
【図14】



【図15】



【図18】



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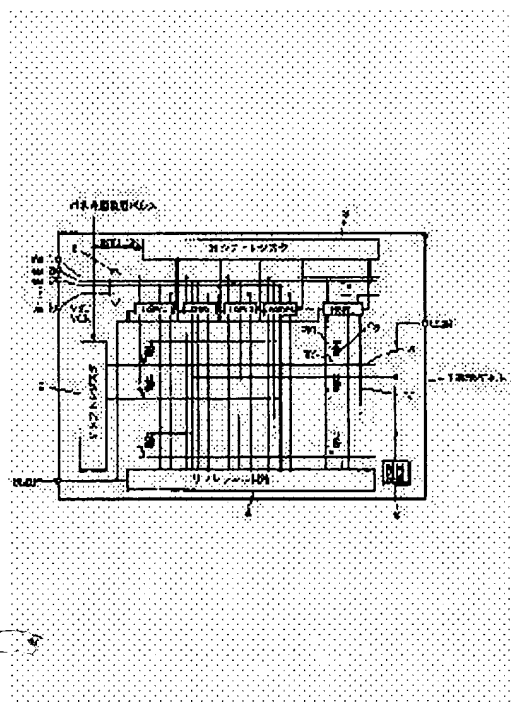
(72)Inventor : GOTO HISASHI

(54) ACTIVE MATRIX DISPLAY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To suppress power consumption as the total of a display system in which an active matrix display device is used in a panel.

SOLUTION: This active matrix display device 1 has row shaped gate lines X, column shaped signal lines Y, matrix shaped pixels PXL arranged at intersections of both lines, a V shift register 2 line sequentially scanning respective gate lines X to select pixels PXL equivalent to one row every one horizontal period and an H shift register 3 sampling video signals sig1-sigk supplied from the outside in one horizontal period to respective signal lines Y to write the video signals of sig1-sigk in the selected pixels PXL equivalent to one row. Moreover, the



device is provided with a refresh circuit 4, which

temporarily separates the signal lines Y from the outside in blanking periods of the video signals sig1-sigk and short circuits plural signal lines Y in which video signal sig1-sigk whose polarities are opposite each other are sampled internally in the blanking periods to neutralize electric charge of respective signal lines Y internally in a state in which they are separated from the outside.

LEGAL STATUS

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CLAIMS

[Claim(s)]

[Claim 1] (41) Color agent 5-amino o-cresol, a 2-amino-4-nitrophenol, A 2-amino-5-nitrophenol, 1-amino-4-methylamino anthraquinone, 3 and 3'-imino diphenol, a hydrochloric acid 2, 4-diamino phenoxyethanol, A hydrochloric acid 2, 4-diaminophenol, hydrochloric-acid toluene -2, 5-diamine, A hydrochloric-acid nitro p phenylenediamine, a hydrochloric-acid p phenylenediamine, A hydrochloric-acid N-phenyl p phenylenediamine, a hydrochloric-acid meta-phenylenediamine, An alt.aminophenol, an acetic-acid N-phenyl p phenylenediamine, 1,4-diaminoanthraquinone, 2, 6-diamino pyridine, 1, 5-dihydroxy naphthalene, Toluene -2, 5-diamine, toluene -3, 4-diamine, a nitro p phenylenediamine, Para-aminophenol, a PARANITORO alt.phenylenediamine, a p phenylenediamine, A PARAME chill aminophenol, a picramic acid, sodium picramate, An N and N'-screw (4-aminophenyl) -2, 5-diamino -1, 4-quinone diimine, 5-(2-hydroxyethylamino)-2-methyl phenol, N-phenyl p phenylenediamine, a meta-aminophenol, a meta-phenylenediamine, sulfuric-acid 5-amino o-cresol, a gate line of behavior A train-like signal line A pixel of a letter of a matrix allotted to each intersection of both A vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period A level actuation circuit which writes a video signal in a pixel for a party which sampled a video signal supplied from the outside to each signal line, and was chosen within a 1 level period It is the active-matrix indicating equipment equipped with the above, and while separating a signal line temporarily from the exterior at a blanking period of a video signal, it is characterized by having a refresh circuit internally neutralized where it short-circuited internally two or more signal lines with which a video signal of antipole nature was sampled mutually in this blanking period and a charge of each signal line is separated from the exterior.

[Claim 2] Said refresh circuit is a active-matrix display according to claim 1 characterized by short-circuiting all signal lines internally while separating all signal lines from the exterior.

[Claim 3] Said refresh circuit is a active-matrix display according to claim 1 characterized by dividing all two or more signal lines into each group, and short-circuiting them by group comrade.

[Claim 4] Said level actuation circuit is a active-matrix display according to claim 1 characterized by sampling a video signal of antipole nature by turns to a signal line arranged in the shape of a train.

[Claim 5] A display system which consists of a video driver which supplies a video signal which polarity reverses to predetermined reference voltage characterized by providing the following, a timing generator which supplies a control signal synchronizing with this video signal, and a display panel which operates according to this control signal and displays an image based on this video signal Said display panel is the gate line of behavior. A train-like signal line A pixel of a letter of a matrix allotted to each intersection of both A vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period, It has a level actuation circuit which writes a video signal in a pixel for a party which sampled a video signal supplied from this external video driver to each signal line, and was chosen within a 1 level period, and displays an image. While separating a signal line from this external video driver temporarily at a blanking period of a video signal according to a control signal supplied from this timing generator A refresh circuit internally neutralized

where it short-circuited internally two or more signal lines with which a video signal of antipole nature was sampled mutually in this blanking period and a charge of each signal line is separated from the exterior

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] This invention relates to the active-matrix display (it may be hereafter called a display panel for short) which contained the pixel which constitutes a screen, switching elements, such as a thin film transistor which drives this, and a surrounding actuation circuit. Moreover, it is related with the display system which consists of the video driver which supplies the video signal which reverses polarity to predetermined reference voltage, a timing generator which supplies a control signal synchronizing with a video signal, and a display panel which operates according to a control signal and displays an image based on a video signal.

[0002]

[Description of the Prior Art] With reference to drawing 15, the conventional active-matrix display is explained briefly. The display panel 1 is equipped with the gate line X of behavior, and the train-like signal line Y, and Pixel PXL is formed in both intersection so that it may illustrate. Pixel PXL consists of the pixel electrode formed in one substrate, a counterelectrode 6 formed in the substrate of another side, and electrooptic material, such as liquid crystal held among both. Switching actuation of each pixel PXL is carried out by the corresponding thin film transistor Tr. Moreover, the auxiliary capacity Cs is formed corresponding to each pixel PXL. The gate electrode of a thin film transistor Tr is connected to the corresponding gate line X, a source electrode is connected to the corresponding signal line Y, and the drain electrode is connected to the corresponding pixel electrode. The display panel 1 is equipped with k input lines 5, and accepts k video signals sig1 and sig2 supplied from an external video driver, ..., sigk, respectively. As for each signal line Y, k are connected to the predetermined input line 5 through the level switch HSW as one unit. In addition to the above configuration, the display panel 1 contains the V shift register 2 and the H shift register 3. The V shift register 2 constitutes a vertical-drive circuit, answers pulses for panel actuation supplied from an external timing generator, such as the vertical start pulse VST and the vertical clock pulse VCK, operates, scans one gate line X at a time sequentially, and chooses a pixel for every line. Pulses for panel actuation, such as the level start pulse HST to which the H shift register 3 is similarly supplied from a timing generator on the other hand, and the level clock pulse HCK, are answered, it operates, and closing motion control of the level switches HSW1 and HSW2 which output a sampling pulse one by one and correspond, ..., the HSWi is carried out, and k signal lines Y are packed as one unit, and are driven. That is, the simultaneous sampling of k video signals sig1, ..., the sigk is carried out at the signal line Y which corresponds, respectively.

[0003] In case starting two or more pixel simultaneous sampling actuation is performed, in order to give the amount of delay corresponding to a pixel pitch beforehand to k video signals sig1 - sigk relatively, the sample hold circuit is established in the video driver. While carrying out sample hold of the k video signals serially and giving relatively the amount of delay corresponding to a pixel pitch, by carrying out closing motion control of the group of k signal lines for the level switch HSW simultaneously as an unit, the number of stages contained in the H shift register 3 which drives this level switch can be reduced, and a configuration can be simplified. In addition, a level actuation circuit consists of HSW1 - HSWi,

and an H shift register 3.

[0004] Drawing 16 is the block diagram showing the conventional display system whole configuration. The display system is equipped with the video driver 8, the display panel 1 shown in drawing 15, and the timing generator (TG) 9. In addition, since a display panel 1 uses liquid crystal (LC) as electrooptic material in many cases, it may be called LCD here. A video driver 8 is changed into the video signal sig which processed the video signal SIG by which an external input is carried out, and was suitable for actuation of LCD1. For example, a video driver 8 performs polarity-reversals processing of a video signal sig in a 1 level period (1H), and outputs the alternating-current-ized video signal sig to LCD1. LCD1 is equipped with the liquid crystal pixel prepared in the gate line of behavior, the train-like signal line, and both intersection as it was shown in drawing 15. Moreover, the vertical-drive circuit and the level actuation circuit are built in. A vertical-drive circuit scans a gate line sequentially, and chooses a pixel. A level actuation circuit writes the alternating current-ized video signal sig in the pixel chosen as every 1H by carrying out the sequential sampling of the alternating current-ized video signal sig at a signal line. A timing generator 9 operates according to a synchronizing signal SINC, supplies the alternating current-ized signal FRP to a video driver 8, and performs timing control of polarity-reversals processing. Moreover, the sample hold signal SHP is supplied to a video driver 8, and delay processing of a video signal sig is controlled. Namely, a video driver 8 carries out delay processing of two or more video signals sig relatively according to the array pitch of a pixel, and supplies them to LCD1. Further, a timing generator 9 supplies pulses for panel actuation, such as HST, HCK, VST, and VCK, to LCD1, and performs motion control of a vertical-drive circuit and a level actuation circuit.

[0005] The video driver 8 consists of buffers BUFF for a clamping circuit CLP, the bright circuit BRT, the gamma correction circuit gamma, the gain circuit GAIN, inverting circuit INV.AMP, the inversion switch SW, sample hold circuit S/H, and load actuation etc.

[0006] With reference to drawing 17, actuation of the display system shown in drawing 16 is explained briefly. The pedestal clamp of the video signal SIG inputted from the outside is carried out in a clamping circuit CLP, and the voltage used as criteria is decided. In order to adjust brightness in the bright circuit BRT, bright control of the signal by which the pedestal clamp was carried out is carried out. The signal by which bright control was carried out performs gamma amendment doubled with the property of LCD1 in the gamma correction circuit gamma. A gain adjustment is performed to the signal of which gamma amendment was done in the gain circuit GAIN. The signal AMPIN by which the gain adjustment was carried out is alternating-current-ized by the inversion switch SW. FRP supplied from a timing generator 9 turns on/controls [off] this inversion switch SW. The alternating-current-ized signal passes along sample hold circuit S/H in order to attach the phase contrast suitable for LCD1 which adopts two or more pixel simultaneous actuation. In addition, this sample hold circuit S/H is controlled by SHP supplied from a timing generator 9. The video signal sig by which sample hold was carried out is supplied to LCD1 through Buffer BUFF. It is written in a pixel the k whole dots by HSW1 by which sequential closing motion control of two or more video signals sig1 - the sigk is carried out like - SHWi which were mentioned above at coincidence. In addition, polarity has reversed the video signal sig supplied to LCD1 to predetermined reference voltage to every 1H so that clearly from drawing 17. This reference voltage is almost equal to the common voltage COM impressed to the counterelectrode 6 shown in drawing 15.

[0007] Drawing 18 expresses typically the polarity of the video signal sig written in each pixel PXL of LCD1. In this example, six video signals sig1-sig6 are written in coincidence the whole 6 pixels as $k = 6$. In addition, Pixel PXL constitutes the matrix of a n line m train as a whole. The so-called dot reversal actuation is used for this example. In the 1st line corresponding to the gate line X1, the polar video signals sig1-sig6 of +-+- are written in six pixels 1-1, 1-2, 1-3, 1-4, 1-5, and 1-6 through signal lines Y1-Y6. In the following line [2nd], the polar video signals sig1-sig6 of -+-+ are written in a pixel 2-1, 2-2, 2-3, 2-4, 2-5, and 2-6. Thus, in dot reversal actuation, the video signal sig of antipole nature is mutually written in alternately to the pixel PXL of nxm.

[0008]

[Problem(s) to be Solved by the Invention] As mentioned above, LCD1 needs alternating current

actuation, in order to prevent deterioration of liquid crystal, and it usually needs to reverse a video signal sig to the common voltage COM. this sake COM, for example, common voltage, -- receiving -- a maximum of -- to write the voltage of V_{max} in Pixel PXL, it is necessary to make the voltage of $2V_{max}$ (es) change at the maximum for every polarity reversals Therefore, the buffer BUFF equipped with the capacity that the voltage of $2V_{max}$ (es) can be made to change at the maximum, between short time is needed for the external video driver 8. In the display system using the conventional LCD, in order to carry out the charge and discharge of the loads, such as this buffer BUFF and Pixel PXL, and a signal line Y, the current of a large quantity is flowing, and this occupied the great portion of power consumption of a display system.

[0009] In order to solve this problem, the load of the pixel set as the object of charge and discharge or a signal line was mitigated, and voltage impressed to a pixel was reduction-ized. However, in the case of the former, there is a physical limit, and it does not necessarily become sufficient cure. Moreover, in the case of the latter, the side effect of image quality deterioration, such as lowering of contrast, had appeared.

[0010]

[Means for Solving the Problem] The following means were provided in order to solve a technical problem of a Prior art mentioned above. Namely, a active-matrix display (display panel) concerning this invention A pixel of a letter of a matrix allotted to a gate line of behavior, a train-like signal line, and each intersection of both as a fundamental configuration, It has a level actuation circuit which writes a video signal in a vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period, and a pixel for a party which sampled a video signal supplied from the outside to each signal line, and was chosen within a 1 level period. As a feature matter, it short-circuits internally two or more signal lines with which a video signal of antipole nature was sampled mutually in this blanking period, and where a charge of each signal line is separated from the exterior, this active-matrix-indicating equipment is internally neutralized, while it is equipped with a refresh circuit and separates a signal-line temporarily from the exterior at a blanking period of a video signal. Preferably, said refresh circuit short-circuits all signal lines internally while separating all signal lines from the exterior. Or said refresh circuit may divide all two or more signal lines into each group, and may be made to short-circuit them by group comrade. In addition, said level actuation circuit samples a video signal of antipole nature by turns to a signal line arranged for example, in the shape of a train.

[0011] This invention includes a display system which used for a display panel a active-matrix indicating equipment mentioned above. This display system consists of a video driver which supplies a video signal which polarity reverses to predetermined reference voltage as a fundamental configuration, a timing generator which supplies a control signal synchronizing with this video signal, and a display panel which operates according to this control signal and displays an image based on this video signal. A pixel of a letter of a matrix matched for a gate line of behavior, a train-like signal line, and each intersection of both with said display panel, A vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period, It has a level actuation circuit which writes a video signal in a pixel for a party which sampled a video signal supplied from this external video driver to each signal line, and was chosen within a 1 level period, and displays an image. As a feature matter, this display panel contains a refresh circuit, and it short-circuits internally two or more signal lines with which a video signal of antipole nature was mutually sampled while separating a signal line from this external video driver temporarily at a blanking period of a video signal according to a control signal supplied from this timing generator in this blanking period, and where a charge of each signal line is separated from the exterior, it neutralizes it internally.

[0012] Usually, display panels, such as LCD, need to carry out the charge and discharge of the twice of voltage written in a pixel in order to reverse a video signal to reference voltage. In this invention, a signal line with which a video signal of straight polarity was sampled inside LCD at a blanking period, and signal line of each other with which a video signal of negative polarity was sampled are short-circuited (short circuit), and a charge is neutralized (cancellation). This reduces a charge which carries

out charge and discharge to a shelf-life, and low-power-ization of a display system is in drawing. When dot reversal actuation is adopted in a active-matrix display panel, specifically, a signal line in a panel is once refreshed on voltage near reference voltage by making all signal lines short-circuit at an image blanking period for every 1 level period. At this time, a signal line in a display panel and an external video driver are refreshed only with a charge inside a panel by dissociating thoroughly. Or in dot reversal actuation, it is also possible to refresh a signal line in a display panel on voltage near reference voltage by making it short-circuit, respectively for every two or more signal lines adjoin an image blanking period for every 1 level period. With the conventional display panel, the charge and discharge of the signal line were carried out to a negative polarity side to reference voltage from a straight polarity or straight polarity side from a negative polarity side by video driver side. According to this invention, since potential of a signal line can be refreshed near reference voltage only with a charge inside a panel, charges and discharges from an external circuit can be reduced substantially, and reduction-izing is possible in power consumption in the whole display system. It is possible to attain low-power-ization, without reduction-izing voltage which reduces loads or is written in a pixel according to this invention. [0013]

[Embodiment of the Invention] With reference to a drawing, the operation gestalt of this invention is explained to details below. Drawing 1 is the circuit diagram showing the fundamental configuration of the active-matrix display (display panel) concerning this invention. In addition, a corresponding reference number is given to the conventional active-matrix display shown in drawing 15, and a corresponding portion, and an understanding is made easy. The so-called two or more pixel-simultaneous actuation method is used for this operation gestalt. However, this invention is not restricted to this and can be applied also to the line sequential color TV system which writes a video signal in the pixel for the dot sequential system which writes in a video signal for every one pixel, or a party by package. The display panel 1 is equipped with the gate line X of behavior, and the train-like signal line Y, and Pixel PXL is formed in both intersection so that it may illustrate. Switching actuation of each pixel PXL is carried out by the corresponding thin film transistor Tr. The gate electrode of a thin film transistor Tr is connected to the corresponding gate line X, a source electrode is connected to the corresponding signal line Y, and the drain electrode is connected to the corresponding pixel electrode. Each pixel electrode has met the counterelectrode 6 and electrooptic material, such as liquid crystal, is held among both. The common voltage COM is impressed to the counterelectrode 6 from the exterior. The display panel 1 is equipped with k input lines 5, and accepts k video signals sig1 supplied from an external video driver - sigk, respectively. As for each signal line Y, k are connected to the predetermined input line 5 through the level switch HSW as one unit. In addition to the above configuration, the display panel 1 contains the V shift register 2 and the H shift register 3. The V shift register 2 answers pulses for panel actuation supplied from an external timing generator, such as the vertical start pulse VST and the vertical clock pulse VCK, operates, scans one gate line X at a time sequentially, and chooses a pixel for every line. That is, the V shift register 2 constitutes a vertical-drive circuit. Pulses for panel actuation, such as the level start pulse HST to which the H shift register 3 is similarly supplied from a timing generator on the other hand, and the level clock pulse HCK, are answered, it operates, and closing motion control of the level switch HSW1 which outputs a sampling pulse one by one and corresponds - the HSWi is carried out, and k signal lines Y are packed as one unit, and are driven. That is, the simultaneous sampling of k video signals sig1 - the sigk is carried out at the signal line Y which corresponds, respectively. A level actuation circuit consists of an H shift register 3 and HSW.

[0014] This display panel 1 is equipped with the refresh circuit 4 as a feature matter. It short-circuits internally two or more signal lines Y with which the video signal sig1 of antipole nature - sigk were sampled mutually in a blanking period, and where the charge of each signal line Y is separated from the exterior, this refresh circuit 4 is internally neutralized, while it operates according to the control signal BLKP supplied from an external timing generator and separates a signal line Y from an external video driver temporarily at the blanking period of a video signal sig1 - sigk. Specifically, the refresh circuit 4 connects each signal line Y electrically within the main-part of the refresh circuit 4 while making an OFF state temporarily the level switch HSW1 - HSWi during a blanking period according to BLKP.

[0015] Drawing 2 shows the concrete example of a configuration of the refresh circuit 4. In the example shown in (A), while separating all the signal lines Y from the exterior, it has the switch RSW for short-circuiting all the signal lines Y internally according to BLKP. On the other hand, in the example of (B), k signal lines Y are divided into each group, for example, and it is short-circuiting each other 2 sets at a time. In addition, this invention is not restricted to this and should just short-circuit the signal line with which the video signal of straight polarity was sampled fundamentally, and the signal line with which the video signal of negative polarity was sampled a same number book every.

[0016] Drawing 3 is the block diagram showing the display system concerning this invention. In addition, in order to make an understanding easy, the corresponding reference number is given to the conventional display system shown in drawing 16, and the corresponding portion. This display system is equipped with the video driver 8, the timing generator 9, and the display panel (LCD) 1 so that it may illustrate. A video driver 8 supplies the video signal sig inverted to predetermined reference voltage. A timing generator 9 supplies the pulse for panel actuation, and a control signal BLKP synchronizing with a video signal sig. LCD1 operates according to the pulse for panel actuation, or a control signal BLKP, and displays an image based on a video signal sig. The pixel of the letter of a matrix matched with LCD1 for the gate line of behavior, a train-like signal line, and each intersection of both like mentioned above, The vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses the pixel for a party for every 1 level period, It has the level actuation circuit which writes a video signal in the pixel for the party which sampled the video signal sig supplied from the external video driver 8 to each signal line, and was chosen within the 1 level period, and displays an image. In addition, the vertical-drive circuit consists of V shift registers, and the level actuation circuit consists of combination of H shift register and the level switch HSW. As a feature matter, LCD1 builds in the refresh circuit. It short-circuits internally two or more signal lines with which the video signal of antipole nature was sampled mutually in a blanking period, and where the charge of each signal line is separated from the exterior, this refresh circuit is internally neutralized, while it separates a signal line from the external video driver 8 temporarily at the blanking period of a video signal sig according to the control signal BLKP supplied from a timing generator 9.

[0017] Drawing 4 is the block diagram showing the example of the display system concerning this invention. This example adopted the 6-pixel simultaneous actuation method ($k = 6$), and has adopted the dot reversal actuation method. A video driver 8 processes a video signal SIG, and supplies six video signals 1-sig 6 to LCD1. sig 1-6 is alternating-current-ized, and phase adjustment is performed. The red video signal is assigned to sig1 and sig2, the green video signal is assigned to sig3 and sig4, and the blue video signal is assigned to sig5 and sig6. A timing generator 9 operates according to a synchronizing signal SYNC, and supplies the alternating current-ized signal FRP and the sample hold signal SHP to the video driver 8. Moreover, the timing generator 9 supplies the pulse for panel actuation and control signals BLKP, such as HST, HCK, VST, and VCK, to LCD1.

[0018] Drawing 5 expresses typically the polarity of each video signal shown in drawing 4. The video signal sig includes the shelf-life and the other blanking period in every 1 level period (1H). A video signal is written for the gate of the thin film transistor corresponding to the pixel for a party in each pixel through an aperture and a signal line within a shelf-life. Polarity reverses video signals sig1, sig3, and sig5 to every 1H to reference voltage. This reference voltage is substantially [as the common voltage COM supplied to the counterelectrode of LCD1] equal. Similarly, polarity also reverses video signals sig2, sig4, and sig6 to every 1H. However, sig 1, 3, and 5 and sig 2, 4, and 6 serve as antipole nature mutually. For example, when its attention is paid to a party eye (the 1st line), sig 1, 3, and 5 has the voltage of +V to COM, and sig 2, 4, and 6 has the voltage of -V to COM.

[0019] Drawing 6 is the circuit diagram showing the concrete configuration of LCD1 shown in drawing 4. Pixel PXL is matrix arrangement of n line xm line so that it may illustrate. Although n gate lines X are not illustrated in total, it connects with V shift register. Moreover, m signal lines Y are connected to six input lines 5 through HSW in total, and sig1-sig6 are sampled, respectively. Closing motion control of each HSW is carried out with the H shift register 3. In this example, since the 6-pixel simultaneous actuation method is adopted, the number of HSW becomes $m/6$. It separates to each HSW, and the

switch CSW of business is built in, each HSW is made into an OFF state according to a control signal BLKP, and a signal line Y and the input line 5 of each other are separated. Moreover, the refresh circuit 4 which built in RSW is connected to the other end side of each signal line Y. This refresh circuit 4 makes all RSW(s) an ON state according to BLKP, and short-circuits all the signal lines Y of each other.

[0020] Next, the actuation of LCD shown in drawing 6 with reference to drawing 7 thru/or drawing 10 is explained to details. As first shown in drawing 7, all of the pixel 1-1 of the 1st line - 1-m are electrically connected to the corresponding signal line Y by turning on altogether the thin film transistor Tr connected with the 1st line. At this time, each CSWs of all built in HSW are supplied to the H shift register 3 side. First, HSW1 will be in switch-on by control of the H shift register 3, and the signal potential of video signals sig1-sig6 is written in a pixel 1-1 to 1-6 at once through six signal lines Y1-Y6 connected with HSW1. Consequently, a pixel 1-1, 1-2, 1-3, 1-4, 1-5, and 1-6 become the polarity of +1+1+, respectively. Subsequently, the potential by which HSW1 was written in the aperture and the pixel 1-1 to 1-6 is held. It is held by the same polar signal potential as the pixel 1-1 to 1-6 to which six signal lines Y1-Y6 connected with HSW1 also correspond at this time.

[0021] Next, as shown in drawing 8, HSW2 will be in switch-on and the polar signal potential of ++-+- is written in a pixel 1-7 to 1-12 through signal lines Y7-Y12. Subsequently, HSW2 will be in non-switch-on, and the polar signal potential of a graphic display is held by the signal lines Y7-Y12 connected with a pixel 1-7 to 1-12, and these. Thus, the predetermined video signals sig1-sig6 are written in and held by the pixel and the signal line every 6 pixels. If signal potential is written in all of the pixels 1-1 of the 1st line - 1-m, the thin film transistor Tr of the 1st line will be in non-switch-on altogether, and will complete the scan for a party.

[0022] Thus, the shelf-life of the 1 level periods expires, and it enters at a blanking period. At this time, as shown in drawing 9, a control signal BLKP inputs from a timing generator, and all HSW(s) are put on an OFF state through CSW. Simultaneously, all RSW(s) in the refresh circuit 4 will be in an ON state, and all the signal lines Y short-circuit mutually. That is, the signal line of the odd number train charged by +V and the signal line of the even number train charged by -V will be in a short circuit condition mutually, and Y will become the potential (COM) of the **all signal-lines 0 neighborhood. Since all HSW(s) are OFF states at this time, receipts and payments of the current from the LCD outside are absolutely none. + When the signal line charged by V and the signal line charged by -V short-circuit, refresh all signal lines in this potential (near COM).

[0023] Next, as shown in drawing 10, the scan of the 2nd line starts. At this time, sig1-sig6 used as reversed polarity are supplied in the 1st line from a video driver. That is, sig 1, 3, and 5 has the potential of -V to COM, and sig 2, 4, and 6 serves as potential of +V to COM. The thin film transistor Tr corresponding to the 2nd line will be in switch-on. Then, sequential closing motion control of the HSW is carried out, and sig1-sig6 are written in the pixel which corresponds through the corresponding signal line Y. Namely, as for the signal line with which sig 1, 3, and 5 was sampled, potential shifts to -V from 0, and, as for the signal line with which sig 2, 4, and 6 was sampled, potential shifts to +V from 0. since the signal line is beforehand refreshed near common voltage altogether -- an external video driver -- each signal line -- V -- charge -- or what is necessary is just to carry out a discharge. Therefore, the power consumed with the buffer in a video driver is substantially reducible compared with the former.

[0024] Although the example mentioned above is the case of dot reversal actuation, this invention is not restricted to this. If the pixel and signal line which are held by straight polarity to the common voltage of LCD paying attention to a certain time amount, and the pixel and signal line which are held by negative polarity exist fundamentally, it cannot be based on the actuation method but this invention can be applied. For example, it is applicable also to the column reversal actuation which samples the video signal of antipole nature by turns the whole train. Moreover, also in the 1H reversal which polarity reverses for every line, it can refresh at a 1 vertical blanking period, for example. It is possible to refresh a request in short-circuiting [in / for the thin film transistor connected with all gate lines at a 1 vertical blanking period / an ON state] all signal lines of each other.

[0025] Drawing 11 is the block diagram showing the example of reference of a active-matrix indicating

equipment. A corresponding reference number is given to the example shown in drawing 6, and a corresponding portion, and an understanding is made easy. This example of reference is not equipped with the refresh function.

[0026] Then, with reference to drawing 12 - drawing 14, actuation of the example of reference shown in drawing 11 is explained briefly. As first shown in drawing 12, when the thin film transistor Tr connected with the 1st line will be in switch-on altogether, all of the pixel 1-1 of the 1st line - 1-m are connected with a signal line Y. Subsequently, when HSW1 closes, signal potential is written in a pixel 1-1 to 1-6 at once through six signal lines Y1-Y6 connected with this. Subsequently, the potential by which HSW1 was written in the aperture and the pixel 1-1 to 1-6 is held. At this time, signal potential is held like [six signal lines Y1-Y6 connected with HSW1] a pixel. That is, signal lines Y1, Y3, and Y5 are charged by +V, and signal lines Y2, Y4, and Y6 are charged by -V.

[0027] Then, as shown in drawing 13, HSW2 will be in switch-on and signal potential is written in a pixel 1-7 to 1-12. Then, HSW2 will be in non-switch-on, and signal potential is held by a pixel 1-7 to 1-12, and signal lines Y7-Y12. Y7, Y9, and Y11 are held by +V, and Y8, Y10, and Y12 are held by -V. Signal potential is written in and held by the pixel and the signal line every 6 pixels like the following. If signal potential is altogether written in the pixel 1-1 of the 1st line - 1-m, the thin film transistor (pixel switch) Tr of the 1st line will be in an OFF state altogether, and will complete the scan of the 1st line.

[0028] As shown in drawing 14 after this, the video signals sig1-sig6 of reversed polarity are supplied in the 1st line from a video driver. sig 1, 3, and 5 serves as potential of negative polarity to COM, and sig 2, 4, and 6 serves as potential of straight polarity to COM. Subsequently, after the thin film transistor Tr of the 2nd line will be in an ON state, sequential closing motion control of the HSW is carried out, and sig1-sig6 are written in the pixel through each signal line. If its attention is paid to signal lines Y1, Y3, and Y5, the potential currently held by +V in the 1st line will be rewritten by -V by the 2nd line. At this time, the buffer by the side of a video driver must perform the discharge of 2V. Moreover, if its attention is paid to signal lines Y2, Y4, and Y6, the potential currently held by -V in the 1st line will be rewritten by +V by the 2nd line. At this time, the buffer by the side of a video driver must charge 2V. Thus, the buffer in a video driver consumes big power.

[0029]

[Effect of the Invention] According to this invention, as explained above, it short-circuits internally two or more signal lines with which the video signal of antipole nature was sampled mutually in a blanking period, and where the charge of each signal line is separated from the exterior, the active-matrix indicating equipment is internally neutralized, while it contains the refresh circuit and separates a signal line temporarily from the exterior at the blanking period of a video signal. With the conventional active-matrix display, the charge and discharge of the potential of a signal line were carried out to the negative side from the positive or positive side from a negative side to common voltage (reference voltage) in the condition of having connected with the exterior. On the other hand, if this invention is used, since signal-line potential can be refreshed near common voltage only with the charge inside a active-matrix display, the charge and discharge from an external circuit can be reduced substantially, and it is possible to reduce the power consumption in the whole display system.

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TECHNICAL FIELD

[A technical field to which invention belongs] This invention relates to a active-matrix display (it may be hereafter called a display panel for short) which contained a pixel which constitutes a screen, switching elements, such as a thin film transistor which drives this, and a surrounding actuation circuit. Moreover, it is related with a display system which consists of a video driver which supplies a video signal which reverses polarity to predetermined reference voltage, a timing generator which supplies a control signal synchronizing with a video signal, and a display panel which operates according to a control signal and displays an image based on a video signal.

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PRIOR ART

[Description of the Prior Art] With reference to drawing 15, the conventional active-matrix display is explained briefly. The display panel 1 is equipped with the gate line X of behavior, and the train-like signal line Y, and Pixel PXL is formed in both intersection so that it may illustrate. Pixel PXL consists of the pixel electrode formed in one substrate, a counterelectrode 6 formed in the substrate of another side, and electrooptic material, such as liquid crystal held among both. Switching actuation of each pixel PXL is carried out by the corresponding thin film transistor Tr. Moreover, the auxiliary capacity Cs is formed corresponding to each pixel PXL. The gate electrode of a thin film transistor Tr is connected to the corresponding gate line X, a source electrode is connected to the corresponding signal line Y, and the drain electrode is connected to the corresponding pixel electrode. The display panel 1 is equipped with k input lines 5, and accepts k video signals sig1 and sig2 supplied from an external video driver, ..., sigk, respectively. As for each signal line Y, k are connected to the predetermined input line 5 through the level switch HSW as one unit. In addition to the above configuration, the display panel 1 contains the V shift register 2 and the H shift register 3. The V shift register 2 constitutes a vertical-drive circuit, answers pulses for panel actuation supplied from an external timing generator, such as the vertical start pulse VST and the vertical clock pulse VCK, operates, scans one gate line X at a time sequentially, and chooses a pixel for every line. Pulses for panel actuation, such as the level start pulse HST to which the H shift register 3 is similarly supplied from a timing generator on the other hand, and the level clock pulse HCK, are answered, it operates, and closing motion control of the level switches HSW1 and HSW2 which output a sampling pulse one by one and correspond, ..., the HSWi is carried out, and k signal lines Y are packed as one unit, and are driven. That is, the simultaneous sampling of k video signals sig1, ..., the sigk is carried out at the signal line Y which corresponds, respectively.

[0003] In case starting two or more pixel simultaneous sampling actuation is performed, in order to give the amount of delay corresponding to a pixel pitch beforehand to k video signals sig1 - sigk relatively, the sample hold circuit is established in the video driver. While carrying out sample hold of the k video signals serially and giving relatively the amount of delay corresponding to a pixel pitch, by carrying out closing motion control of the group of k signal lines for the level switch HSW simultaneously as an unit, the number of stages contained in the H shift register 3 which drives this level switch can be reduced, and a configuration can be simplified. In addition, a level actuation circuit consists of HSW1 - HSWi, and an H shift register 3.

[0004] Drawing 16 is the block diagram showing the conventional display system whole configuration. The display system is equipped with the video driver 8, the display panel 1 shown in drawing 15, and the timing generator (TG) 9. In addition, since a display panel 1 uses liquid crystal (LC) as electrooptic material in many cases, it may be called LCD here. A video driver 8 is changed into the video signal sig which processed the video signal SIG by which an external input is carried out, and was suitable for actuation of LCD1. For example, a video driver 8 performs polarity-reversals processing of a video signal sig in a 1 level period (1H), and outputs the alternating-current-ized video signal sig to LCD1. LCD1 is equipped with the liquid crystal pixel prepared in the gate line of behavior, the train-like signal line, and both intersection as it was shown in drawing 15. Moreover, the vertical-drive circuit and the

level actuation circuit are built in. A vertical-drive circuit scans a gate line sequentially, and chooses a pixel. A level actuation circuit writes the alternating current-ized video signal sig in the pixel chosen as every 1H by carrying out the sequential sampling of the alternating current-ized video signal sig at a signal line. A timing generator 9 operates according to a synchronizing signal SINC, supplies the alternating current-ized signal FRP to a video driver 8, and performs timing control of polarity-reversals processing. Moreover, the sample hold signal SHP is supplied to a video driver 8, and delay processing of a video signal sig is controlled. Namely, a video driver 8 carries out delay processing of two or more video signals sig relatively according to the array pitch of a pixel, and supplies them to LCD1. Further, a timing generator 9 supplies pulses for panel actuation, such as HST, HCK, VST, and VCK, to LCD1, and performs motion control of a vertical-drive circuit and a level actuation circuit.

[0005] The video driver 8 consists of buffers BUFF for a clamping circuit CLP, the bright circuit BRT, the gamma correction circuit gamma, the gain circuit GAIN, inverting circuit INV.AMP, the inversion switch SW, sample hold circuit S/H, and load actuation etc.

[0006] With reference to drawing 17, actuation of the display system shown in drawing 16 is explained briefly. The pedestal clamp of the video signal SIG inputted from the outside is carried out in a clamping circuit CLP, and the voltage used as criteria is decided. In order to adjust brightness in the bright circuit BRT, bright control of the signal by which the pedestal clamp was carried out is carried out. The signal by which bright control was carried out performs gamma amendment doubled with the property of LCD1 in the gamma correction circuit gamma. A gain adjustment is performed to the signal of which gamma amendment was done in the gain circuit GAIN. The signal AMPIN by which the gain adjustment was carried out is alternating-current-ized by the inversion switch SW. FRP supplied from a timing generator 9 turns on/controls [off] this inversion switch SW. The alternating-current-ized signal passes along sample hold circuit S/H in order to attach the phase contrast suitable for LCD1 which adopts two or more pixel simultaneous actuation. In addition, this sample hold circuit S/H is controlled by SHP supplied from a timing generator 9. The video signal sig by which sample hold was carried out is supplied to LCD1 through Buffer BUFF. It is written in a pixel the k whole dots by HSW1 by which sequential closing motion control of two or more video signals sig1 - the sigk is carried out like - SHWi which were mentioned above at coincidence. In addition, polarity has reversed the video signal sig supplied to LCD1 to predetermined reference voltage to every 1H so that clearly from drawing 17. This reference voltage is almost equal to the common voltage COM impressed to the counterelectrode 6 shown in drawing 15.

[0007] Drawing 18 expresses typically the polarity of the video signal sig written in each pixel PXL of LCD1. In this example, six video signals sig1-sig6 are written in coincidence the whole 6 pixels as $k=6$. In addition, Pixel PXL constitutes the matrix of a n line m train as a whole. The so-called dot reversal actuation is used for this example. In the 1st line corresponding to the gate line X1, the polar video signals sig1-sig6 of +-+-+ are written in six pixels 1-1, 1-2, 1-3, 1-4, 1-5, and 1-6 through signal lines Y1-Y6. In the following line [2nd], the polar video signals sig1-sig6 of -+-+-+ are written in a pixel 2-1, 2-2, 2-3, 2-4, 2-5, and 2-6. Thus, in dot reversal actuation, the video signal sig of antipole nature is mutually written in alternately to the pixel PXL of nxm.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, as explained above, it short-circuits internally two or more signal lines with which the video signal of antipole nature was sampled mutually in a blanking period, and where the charge of each signal line is separated from the exterior, the active-matrix indicating equipment is internally neutralized, while it contains the refresh circuit and separates a signal line temporarily from the exterior at the blanking period of a video signal. With the conventional active-matrix display, the charge and discharge of the potential of a signal line were carried out to the negative side from the positive or positive side from a negative side to common voltage (reference voltage) in the condition of having connected with the exterior. On the other hand, if this invention is used, since signal-line potential can be refreshed near common voltage only with the charge inside a active-matrix display, the charge and discharge from an external circuit can be reduced substantially, and it is possible to reduce the power consumption in the whole display system.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] As mentioned above, LCD1 needs alternating current actuation, in order to prevent deterioration of liquid crystal, and it usually needs to reverse a video signal sig to the common voltage COM. this sake COM, for example, common voltage, -- receiving -- a maximum of -- to write the voltage of V_{max} in Pixel PXL, it is necessary to make the voltage of $2V_{max}$ (es) change at the maximum for every polarity reversals Therefore, the buffer BUFF equipped with the capacity that the voltage of $2V_{max}$ (es) can be made to change at the maximum, between short time is needed for the external video driver 8. In the display system using the conventional LCD, in order to carry out the charge and discharge of the loads, such as this buffer BUFF and Pixel PXL, and a signal line Y, the current of a large quantity is flowing, and this occupied the great portion of power consumption of a display system.

[0009] In order to solve this problem, the load of the pixel set as the object of charge and discharge or a signal line was mitigated, and voltage impressed to a pixel was reduction-ized. However, in the case of the former, there is a physical limit, and it does not necessarily become sufficient cure. Moreover, in the case of the latter, the side effect of image quality deterioration, such as lowering of contrast, had appeared.

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MEANS

[Means for Solving the Problem] The following means were provided in order to solve a technical problem of a Prior art mentioned above. Namely, a active-matrix display (display panel) concerning this invention A pixel of a letter of a matrix allotted to a gate line of behavior, a train-like signal line, and each intersection of both as a fundamental configuration, It has a level actuation circuit which writes a video signal in a vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period, and a pixel for a party which sampled a video signal supplied from the outside to each signal line, and was chosen within a 1 level period. As a feature matter, it short-circuits internally two or more signal lines with which a video signal of antipole nature was sampled mutually in this blanking period, and where a charge of each signal line is separated from the exterior, this active-matrix indicating equipment is internally neutralized, while it is equipped with a refresh circuit and separates a signal line temporarily from the exterior at a blanking period of a video signal. Preferably, said refresh circuit short-circuits all signal lines internally while separating all signal lines from the exterior. Or said refresh circuit may divide all two or more signal lines into each group, and may be made to short-circuit them by group comrade. In addition, said level actuation circuit samples a video signal of antipole nature by turns to a signal line arranged for example, in the shape of a train.

[0011] This invention includes a display system which used for a display panel a active-matrix indicating equipment mentioned above. This display system consists of a video driver which supplies a video signal which polarity reverses to predetermined reference voltage as a fundamental configuration, a timing generator which supplies a control signal synchronizing with this video signal, and a display panel which operates according to this control signal and displays an image based on this video signal. A pixel of a letter of a matrix matched for a gate line of behavior, a train-like signal line, and each intersection of both with said display panel, A vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period, It has a level actuation circuit which writes a video signal in a pixel for a party which sampled a video signal supplied from this external video driver to each signal line, and was chosen within a 1 level period, and displays an image. As a feature matter, this display panel contains a refresh circuit, and it short-circuits internally two or more signal lines with which a video signal of antipole nature was mutually sampled while separating a signal line from this external video driver temporarily at a blanking period of a video signal according to a control signal supplied from this timing generator in this blanking period, and where a charge of each signal line is separated from the exterior, it neutralizes it internally.

[0012] Usually, display panels, such as LCD, need to carry out the charge and discharge of the twice of voltage written in a pixel in order to reverse a video signal to reference voltage. In this invention, a signal line with which a video signal of straight polarity was sampled inside LCD at a blanking period, and signal line of each other with which a video signal of negative polarity was sampled are short-circuited (short circuit), and a charge is neutralized (cancellation). This reduces a charge which carries out charge and discharge to a shelf-life, and low-power-ization of a display system is in drawing. When dot reversal actuation is adopted in a active-matrix display panel, specifically, a signal line in a panel is

once refreshed on voltage near reference voltage by making all signal lines short-circuit at an image blanking period for every 1 level period. At this time, a signal line in a display panel and an external video driver are refreshed only with a charge inside a panel by dissociating thoroughly. Or in dot reversal actuation, it is also possible to refresh a signal line in a display panel on voltage near reference voltage by making it short-circuit, respectively for every two or more signal lines adjoin an image blanking period for every 1 level period. With the conventional display panel, the charge and discharge of the signal line were carried out to a negative polarity side to reference voltage from a straight polarity or straight polarity side from a negative polarity side by video driver side. According to this invention, since potential of a signal line can be refreshed near reference voltage only with a charge inside a panel, charges and discharges from an external circuit can be reduced substantially, and reduction-izing is possible in power consumption in the whole display system. It is possible to attain low-power-ization, without reduction-izing voltage which reduces loads or is written in a pixel according to this invention. [0013]

[Embodiment of the Invention] With reference to a drawing, the operation gestalt of this invention is explained to details below. Drawing 1 is the circuit diagram showing the fundamental configuration of the active-matrix display (display panel) concerning this invention. In addition, a corresponding reference number is given to the conventional active-matrix display shown in drawing.15, and a corresponding portion, and an understanding is made easy. The so-called two or more pixel simultaneous actuation method is used for this operation gestalt. However, this invention is not restricted to this and can be applied also to the line sequential color TV system which writes a video signal in the pixel for the dot sequential system which writes in a video signal for every one pixel, or a party by package. The display panel 1 is equipped with the gate line X of behavior, and the train-like signal line Y, and Pixel PXL is formed in both intersection so that it may illustrate. Switching actuation of each pixel PXL is carried out by the corresponding thin film transistor Tr. The gate electrode of a thin film transistor Tr is connected to the corresponding gate line X, a source electrode is connected to the corresponding signal line Y, and the drain electrode is connected to the corresponding pixel electrode. Each pixel electrode has met the counterelectrode 6 and electrooptic material, such as liquid crystal, is held among both. The common voltage COM is impressed to the counterelectrode 6 from the exterior. The display panel 1 is equipped with k input lines 5, and accepts k video signals sig1 supplied from an external video driver - sigk, respectively. As for each signal line Y, k are connected to the predetermined input line 5 through the level switch HSW as one unit. In addition to the above configuration, the display panel 1 contains the V shift register 2 and the H shift register 3. The V shift register 2 answers pulses for panel actuation supplied from an external timing generator, such as the vertical start pulse VST and the vertical clock pulse VCK, operates, scans one gate line X at a time sequentially, and chooses a pixel for every line. That is, the V shift register 2 constitutes a vertical-drive circuit. Pulses for panel actuation, such as the level start pulse HST to which the H shift register 3 is similarly supplied from a timing generator on the other hand, and the level clock pulse HCK, are answered, it operates, and closing motion control of the level switch HSW1 which outputs a sampling pulse one by one and corresponds - the HSWi is carried out, and k signal lines Y are packed as one unit, and are driven. That is, the simultaneous sampling of k video signals sig1 - the sigk is carried out at the signal line Y which corresponds, respectively. A level actuation circuit consists of an H shift register 3 and HSW.

[0014] This display panel 1 is equipped with the refresh circuit 4 as a feature matter. It short-circuits internally two or more signal lines Y with which the video signal sig1 of antipole nature - sigk were sampled mutually in a blanking period, and where the charge of each signal line Y is separated from the exterior, this refresh circuit 4 is internally neutralized, while it operates according to the control signal BLKP supplied from an external timing generator and separates a signal line Y from an external video driver temporarily at the blanking period of a video signal sig1 - sigk. Specifically, the refresh circuit 4 connects each signal line Y electrically within the main part of the refresh circuit 4 while making an OFF state temporarily the level switch HSW1 - HSWi during a blanking period according to BLKP.

[0015] Drawing 2 shows the concrete example of a configuration of the refresh circuit 4. In the example shown in (A), while separating all the signal lines Y from the exterior, it has the switch RSW for short-

circuiting all the signal lines Y internally according to BLKP. On the other hand, in the example of (B), k signal lines Y are divided into each group, for example, and it is short-circuiting each other 2 sets at a time. In addition, this invention is not restricted to this and should just short-circuit the signal line with which the video signal of straight polarity was sampled fundamentally, and the signal line with which the video signal of negative polarity was sampled a same number book every.

[0016] Drawing 3 is the block diagram showing the display system concerning this invention. In addition, in order to make an understanding easy, the corresponding reference number is given to the conventional display system shown in drawing 16, and the corresponding portion. This display system is equipped with the video driver 8, the timing generator 9, and the display panel (LCD) 1 so that it may illustrate. A video driver 8 supplies the video signal sig inverted to predetermined reference voltage. A timing generator 9 supplies the pulse for panel actuation, and a control signal BLKP synchronizing with a video signal sig. LCD1 operates according to the pulse for panel actuation, or a control signal BLKP, and displays an image based on a video signal sig. The pixel of the letter of a matrix matched with LCD1 for the gate line of behavior, a train-like signal line, and each intersection of both like mentioned above, The vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses the pixel for a party for every 1 level period, It has the level actuation circuit which writes a video signal in the pixel for the party which sampled the video signal sig supplied from the external video driver 8 to each signal line, and was chosen within the 1 level period, and displays an image. In addition, the vertical-drive circuit consists of V shift registers, and the level actuation circuit consists of combination of H shift register and the level switch HSW. As a feature matter, LCD1 builds in the refresh circuit. It short-circuits internally two or more signal lines with which the video signal of antipole nature was sampled mutually in a blanking period, and where the charge of each signal line is separated from the exterior, this refresh circuit is internally neutralized, while it separates a signal line from the external video driver 8 temporarily at the blanking period of a video signal sig according to the control signal BLKP supplied from a timing generator 9.

[0017] Drawing 4 is the block diagram showing the example of the display system concerning this invention. This example adopted the 6-pixel simultaneous actuation method ($k=6$), and has adopted the dot reversal actuation method. A video driver 8 processes a video signal SIG, and supplies six video signals 1-sig 6 to LCD1. sig 1-6 is alternating-current-ized, and phase adjustment is performed. The red video signal is assigned to sig1 and sig2, the green video signal is assigned to sig3 and sig4, and the blue video signal is assigned to sig5 and sig6. A timing generator 9 operates according to a synchronizing signal SYNC, and supplies the alternating current-ized signal FRP and the sample hold signal SHP to the video driver 8. Moreover, the timing generator 9 supplies the pulse for panel actuation and control signals BLKP, such as HST, HCK, VST, and VCK, to LCD1.

[0018] Drawing 5 expresses typically the polarity of each video signal shown in drawing 4. The video signal sig includes the shelf-life and the other blanking period in every 1 level period (1H). A video signal is written for the gate of the thin film transistor corresponding to the pixel for a party in each pixel through an aperture and a signal line within a shelf-life. Polarity reverses video signals sig1, sig3, and sig5 to every 1H to reference voltage. This reference voltage is substantially [as the common voltage COM supplied to the counterelectrode of LCD1] equal. Similarly, polarity also reverses video signals sig2, sig4, and sig6 to every 1H. However, sig 1, 3, and 5 and sig 2, 4, and 6 serve as antipole nature mutually. For example, when its attention is paid to a party eye (the 1st line), sig 1, 3, and 5 has the voltage of +V to COM, and sig 2, 4, and 6 has the voltage of -V to COM.

[0019] Drawing 6 is the circuit diagram showing the concrete configuration of LCD1 shown in drawing 4. Pixel PXL is matrix arrangement of n line xm line so that it may illustrate. Although n gate lines X are not illustrated in total, it connects with V shift register. Moreover, m signal lines Y are connected to six input lines 5 through HSW in total, and sig1-sig6 are sampled, respectively. Closing motion control of each HSW is carried out with the H shift register 3. In this example, since the 6-pixel simultaneous actuation method is adopted, the number of HSW becomes m/6. It separates to each HSW, and the switch CSW of business is built in, each HSW is made into an OFF state according to a control signal BLKP, and a signal line Y and the input line 5 of each other are separated. Moreover, the refresh circuit

4 which built in RSW is connected to the other end side of each signal line Y. This refresh circuit 4 makes all RSW(s) an ON state according to BLKP, and short-circuits all the signal lines Y of each other.

[0020] Next, the actuation of LCD shown in drawing 6 with reference to drawing 7 thru/or drawing 10 is explained to details. As first shown in drawing 7, all of the pixel 1-1 of the 1st line - 1-m are electrically connected to the corresponding signal line Y by turning on altogether the thin film transistor Tr connected with the 1st line. At this time, each CSWs of all built in HSW are supplied to the H shift register 3 side. First, HSW1 will be in switch-on by control of the H shift register 3, and the signal potential of video signals sig1-sig6 is written in a pixel 1-1 to 1-6 at once through six signal lines Y1-Y6 connected with HSW1. Consequently, a pixel 1-1, 1-2, 1-3, 1-4, 1-5, and 1-6 become the polarity of +1+1+, respectively. Subsequently, the potential by which HSW1 was written in the aperture and the pixel 1-1 to 1-6 is held. It is held by the same polar signal potential as the pixel 1-1 to 1-6 to which six signal lines Y1-Y6 connected with HSW1 also correspond at this time.

[0021] Next, as shown in drawing 8, HSW2 will be in switch-on and the polar signal potential of +--+ is written in a pixel 1-7 to 1-12 through signal lines Y7-Y12. Subsequently, HSW2 will be in non-switch-on, and the polar signal potential of a graphic display is held by the signal lines Y7-Y12 connected with a pixel 1-7 to 1-12, and these. Thus, the predetermined video signals sig1-sig6 are written in and held by the pixel and the signal line every 6 pixels. If signal potential is written in all of the pixels 1-1 of the 1st line - 1-m, the thin film transistor Tr of the 1st line will be in non-switch-on altogether, and will complete the scan for a party.

[0022] Thus, the shelf-life of the 1 level periods expires, and it enters at a blanking period. At this time, as shown in drawing 9, a control signal BLKP inputs from a timing generator, and all HSW(s) are put on an OFF state through CSW. Simultaneously, all RSW(s) in the refresh circuit 4 will be in an ON state, and all the signal lines Y short-circuit mutually. That is, the signal line of the odd number train charged by +V and the signal line of the even number train charged by -V will be in a short circuit condition mutually, and Y will become the potential (COM) of the **all signal-lines 0 neighborhood. Since all HSW(s) are OFF states at this time, receipts and payments of the current from the LCD outside are absolutely none. + When the signal line charged by V and the signal line charged by -V short-circuit, refresh all signal lines in this potential (near COM).

[0023] Next, as shown in drawing 10, the scan of the 2nd line starts. At this time, sig1-sig6 used as reversed polarity are supplied in the 1st line from a video driver. That is, sig 1, 3, and 5 has the potential of -V to COM, and sig 2, 4, and 6 serves as potential of +V to COM. The thin film transistor Tr corresponding to the 2nd line will be in switch-on. Then, sequential closing motion control of the HSW is carried out, and sig1-sig6 are written in the pixel which corresponds through the corresponding signal line Y. Namely, as for the signal line with which sig 1, 3, and 5 was sampled, potential shifts to -V from 0, and, as for the signal line with which sig 2, 4, and 6 was sampled, potential shifts to +V from 0. since the signal line is beforehand refreshed near common voltage altogether -- an external video driver -- each signal line -- V -- charge -- or what is necessary is just to carry out a discharge Therefore, the power consumed with the buffer in a video driver is substantially reducible compared with the former.

[0024] Although the example mentioned above is the case of dot reversal actuation, this invention is not restricted to this. If the pixel and signal line which are held by straight polarity to the common voltage of LCD paying attention to a certain time amount, and the pixel and signal line which are held by negative polarity exist fundamentally, it cannot be based on the actuation method but this invention can be applied. For example, it is applicable also to the column reversal actuation which samples the video signal of antipole nature by turns the whole train. Moreover, also in the 1H reversal which polarity reverses for every line, it can refresh at a 1 vertical blanking period, for example. It is possible to refresh a request in short-circuiting [in / for the thin film transistor connected with all gate lines at a 1 vertical blanking period / an ON state] all signal lines of each other.

[0025] Drawing 11 is the block diagram showing the example of reference of a active-matrix indicating equipment. A corresponding reference number is given to the example shown in drawing 6, and a corresponding portion, and an understanding is made easy. This example of reference is not equipped

with the refresh function.

[0026] Then, with reference to drawing 12 - drawing 14, actuation of the example of reference shown in drawing 11 is explained briefly. As first shown in drawing 12, when the thin film transistor Tr connected with the 1st line will be in switch-on altogether, all of the pixel 1-1 of the 1st line - 1-m are connected with a signal line Y. Subsequently, when HSW1 closes, signal potential is written in a pixel 1-1 to 1-6 at once through six signal lines Y1-Y6 connected with this. Subsequently, the potential by which HSW1 was written in the aperture and the pixel 1-1 to 1-6 is held. At this time, signal potential is held like [six signal lines Y1-Y6 connected with HSW1] a pixel. That is, signal lines Y1, Y3, and Y5 are charged by +V, and signal lines Y2, Y4, and Y6 are charged by -V.

[0027] Then, as shown in drawing 13, HSW2 will be in switch-on and signal potential is written in a pixel 1-7 to 1-12. Then, HSW2 will be in non-switch-on, and signal potential is held by a pixel 1-7 to 1-12, and signal lines Y7-Y12. Y7, Y9, and Y11 are held by +V, and Y8, Y10, and Y12 are held by -V. Signal potential is written in and held by the pixel and the signal line every 6 pixels like the following. If signal potential is altogether written in the pixel 1-1 of the 1st line - 1-m, the thin film transistor (pixel switch) Tr of the 1st line will be in an OFF state altogether, and will complete the scan of the 1st line.

[0028] As shown in drawing 14 after this, the video signals sig1-sig6 of reversed polarity are supplied in the 1st line from a video driver. sig 1, 3, and 5 serves as potential of negative polarity to COM, and sig 2, 4, and 6 serves as potential of straight polarity to COM. Subsequently, after the thin film transistor Tr of the 2nd line will be in an ON state, sequential closing motion control of the HSW is carried out, and sig1-sig6 are written in the pixel through each signal line. If its attention is paid to signal lines Y1, Y3, and Y5, the potential currently held by +V in the 1st line will be rewritten by -V by the 2nd line. At this time, the buffer by the side of a video driver must perform the discharge of 2V. Moreover, if its attention is paid to signal lines Y2, Y4, and Y6, the potential currently held by -V in the 1st line will be rewritten by +V by the 2nd line. At this time, the buffer by the side of a video driver must charge 2V. Thus, the buffer in a video driver consumes big power.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the circuit diagram showing the operation gestalt of the active-matrix display concerning this invention.

[Drawing 2] It is the circuit diagram showing the concrete configuration of the refresh circuit included in the operation gestalt shown in drawing 1.

[Drawing 3] It is the block diagram showing the whole display system configuration concerning this invention.

[Drawing 4] It is the block diagram showing the example of the display system concerning this invention.

[Drawing 5] It is the timing chart with which explanation of the example shown in drawing 4 of operation is presented.

[Drawing 6] It is the circuit diagram showing the concrete configuration of the active-matrix display contained in the example shown in drawing 4.

[Drawing 7] It is the circuit diagram with which explanation of the active-matrix display shown in drawing 6 of operation is presented.

[Drawing 8] It is the circuit diagram with which explanation of the active-matrix display shown in drawing 6 of operation is presented.

[Drawing 9] It is the circuit diagram with which explanation of the active-matrix display shown in drawing 6 of operation is presented.

[Drawing 10] It is the circuit diagram with which explanation of the active-matrix display shown in drawing 6 of operation is presented.

[Drawing 11] It is the circuit diagram showing the example of reference of a active-matrix display.

[Drawing 12] It is the circuit diagram with which explanation of the example of reference shown in drawing 11 of operation is presented.

[Drawing 13] It is the circuit diagram with which explanation of the example of reference shown in drawing 11 of operation is presented.

[Drawing 14] It is the circuit diagram with which explanation of the example of reference shown in drawing 11 of operation is presented.

[Drawing 15] It is the circuit diagram showing an example of the conventional active-matrix display.

[Drawing 16] It is the block diagram showing an example of the conventional display system.

[Drawing 17] It is the wave form chart with which explanation of the conventional display system shown in drawing 16 of operation is presented.

[Drawing 18] It is the mimetic diagram with which explanation of the conventional active-matrix display shown in drawing 15 of operation is presented.

[Description of Notations]

1 [... A refresh circuit, 5 / ... An input line, 6 / ... A counterelectrode, 8 / ... A video driver, 9 / ... Timing generator] ... A display panel, 2 ... V shift register, 3 ... H shift register, 4

[Translation done.]

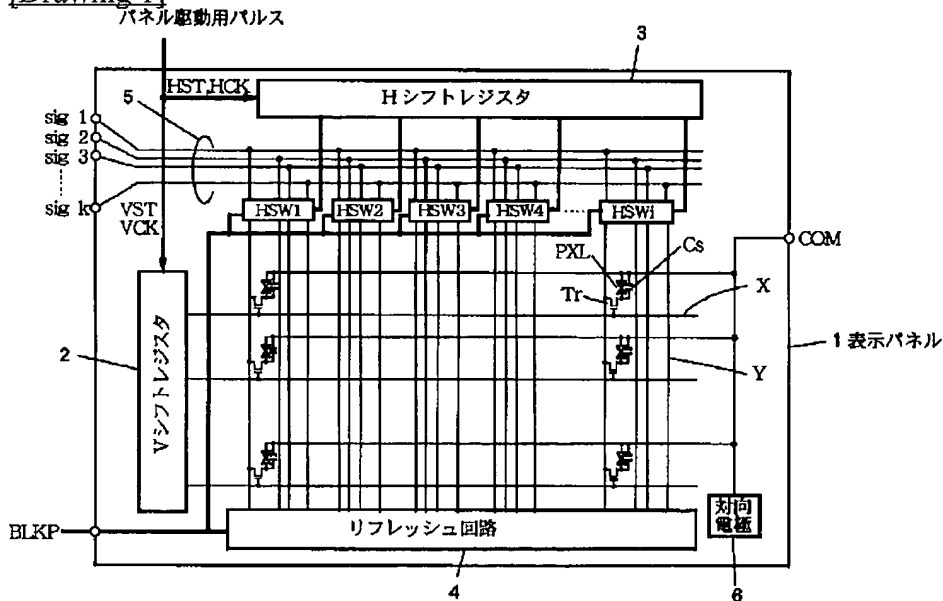
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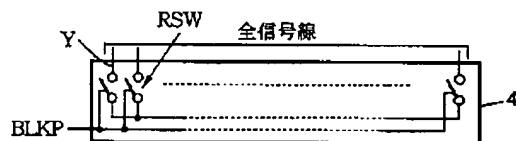
DRAWINGS

[Drawing 1]

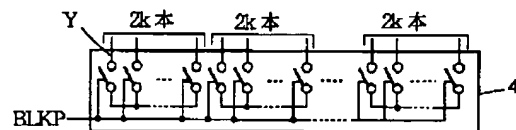


[Drawing 2]

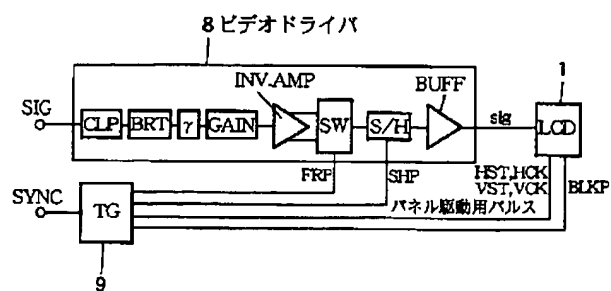
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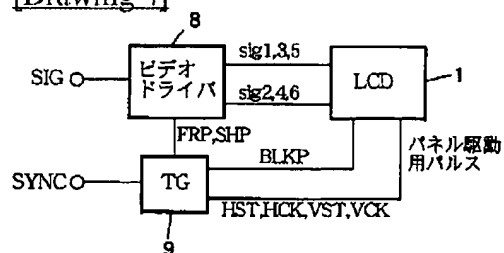
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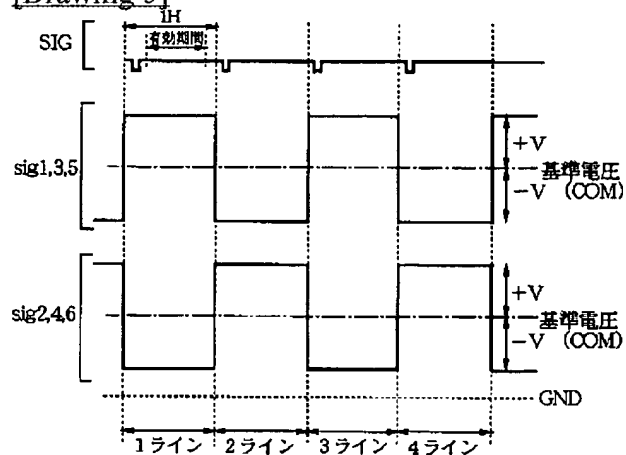
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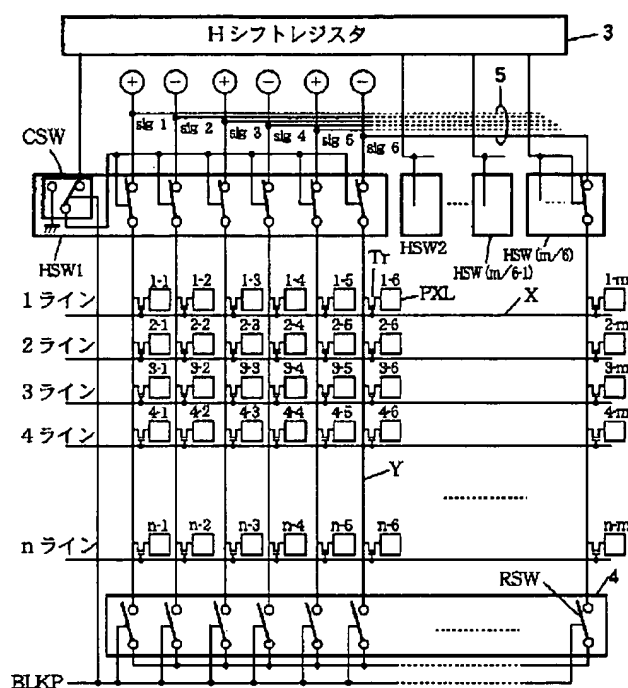
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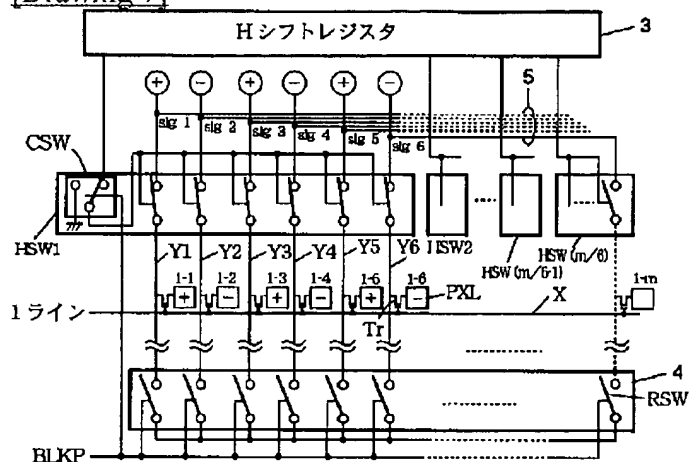
[Drawing 5]



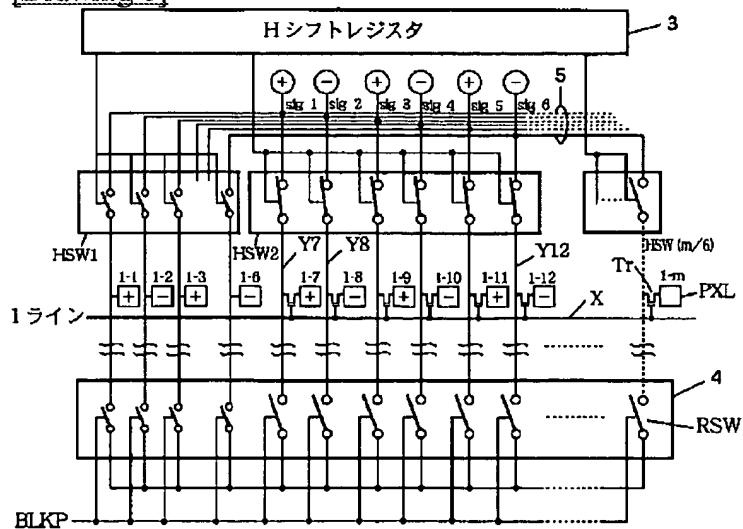
[Drawing 6]

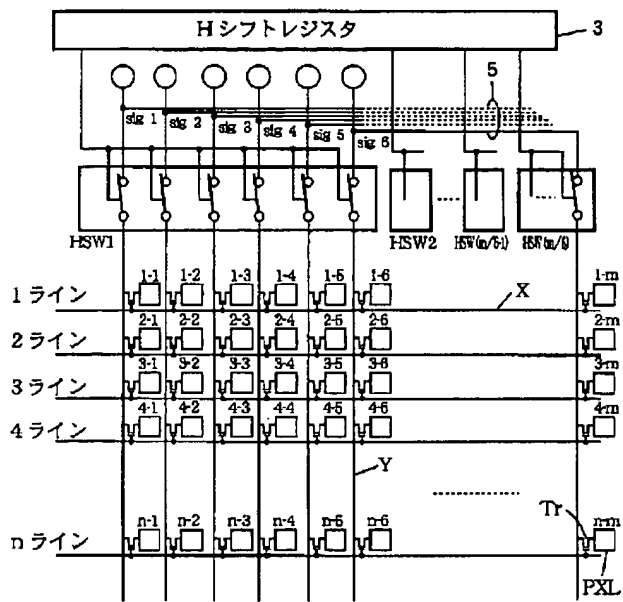


[Drawing 7]

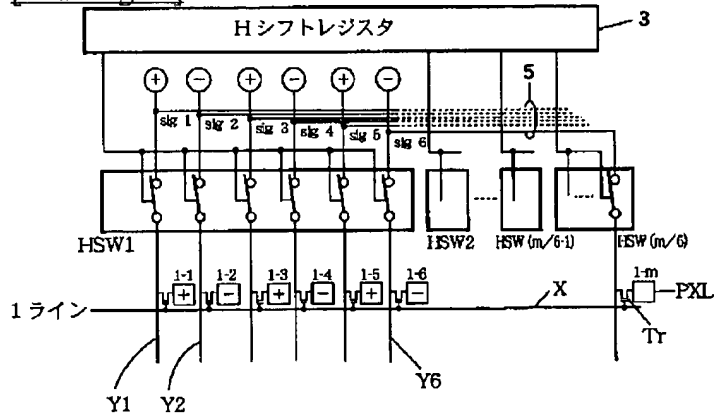


[Drawing 8]

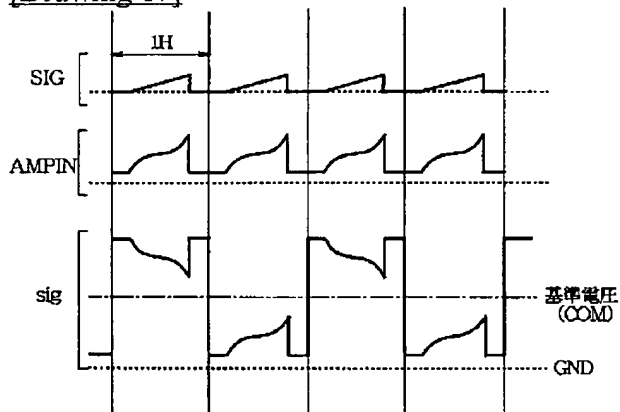




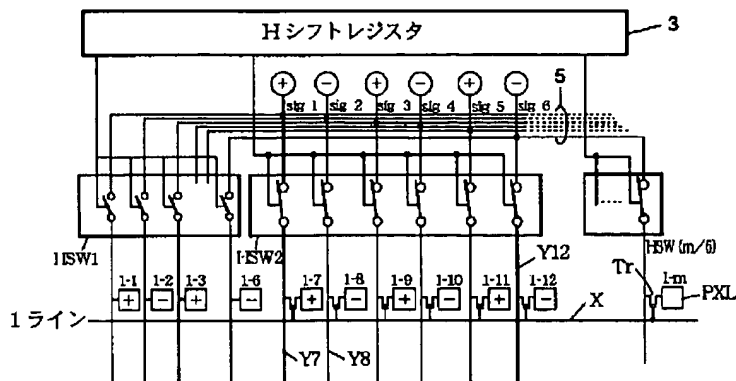
[Drawing 12]



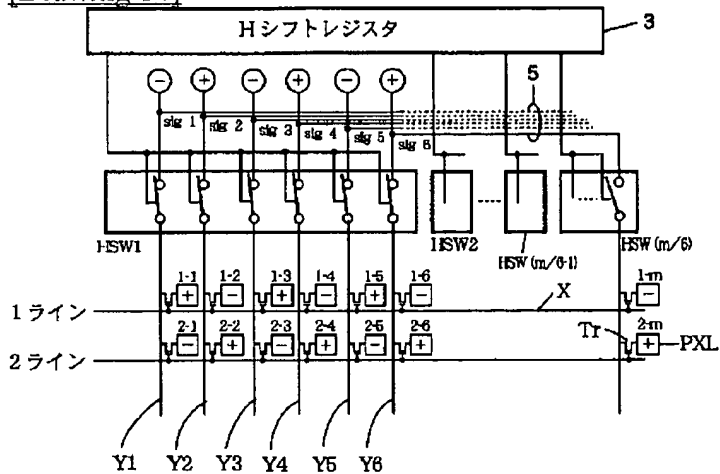
[Drawing 17]



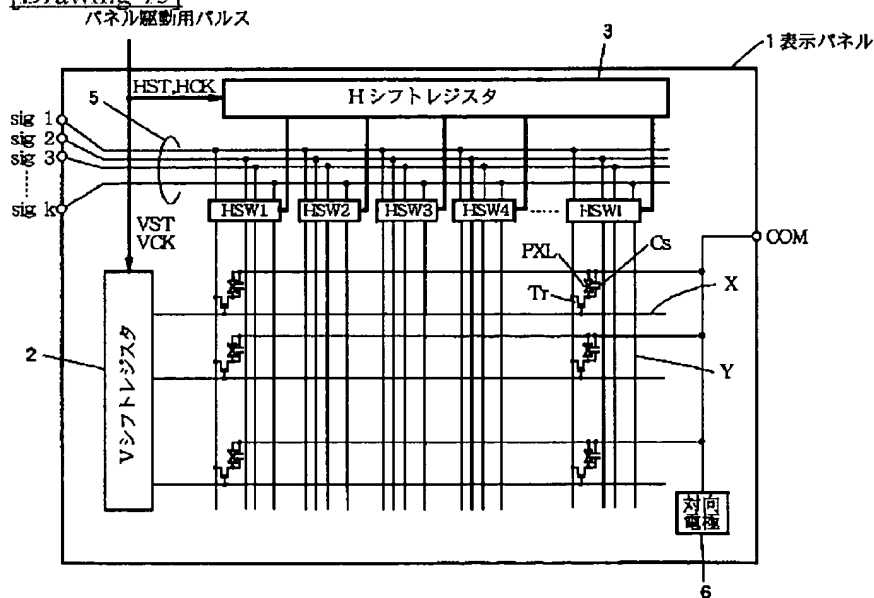
[Drawing 13]



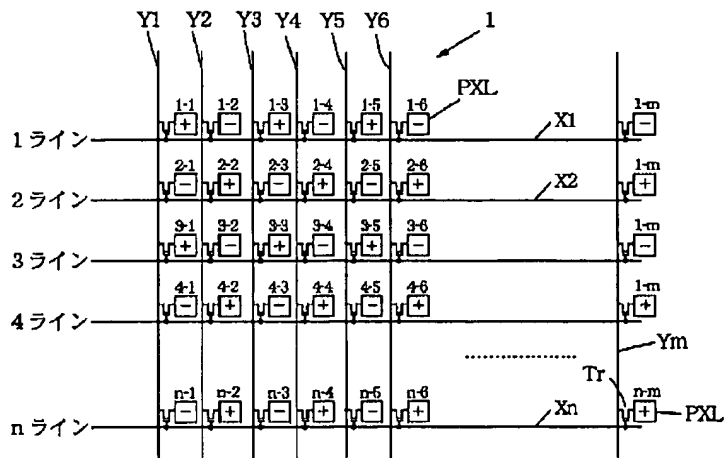
[Drawing 14]



[Drawing 15]



[Drawing 18]



[Translation done.]